DATA SHEET

(DOC No. HX8837-A-DS)

HX8837-A

Display Controller with TTL Input and DETTL Output

Preliminary version 01 March, 2007

Himax Technologies, Inc.
http://www.himax.com.tw

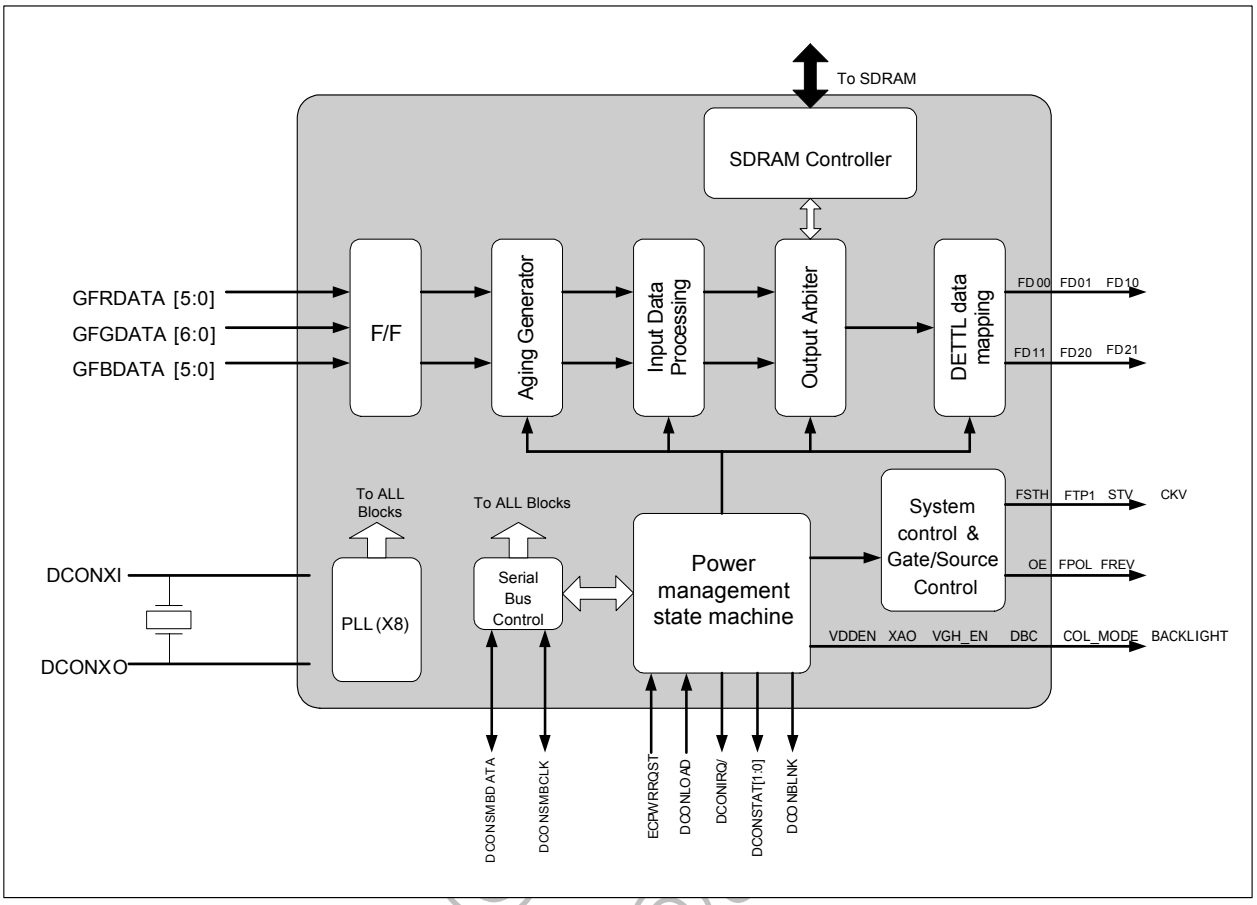
1. General Description

The HX8837-A (The DCON Applications-Specific Integrated Circuit) is a Display Controller that is optimized for driving the One Laptop per Child (OLPC) hybrid color/monochrome 1200x900 TFT display panel. The interfaces of HX8837-A include TTL input (676), 512Kx16 bits SD-RAM and DETTL output.

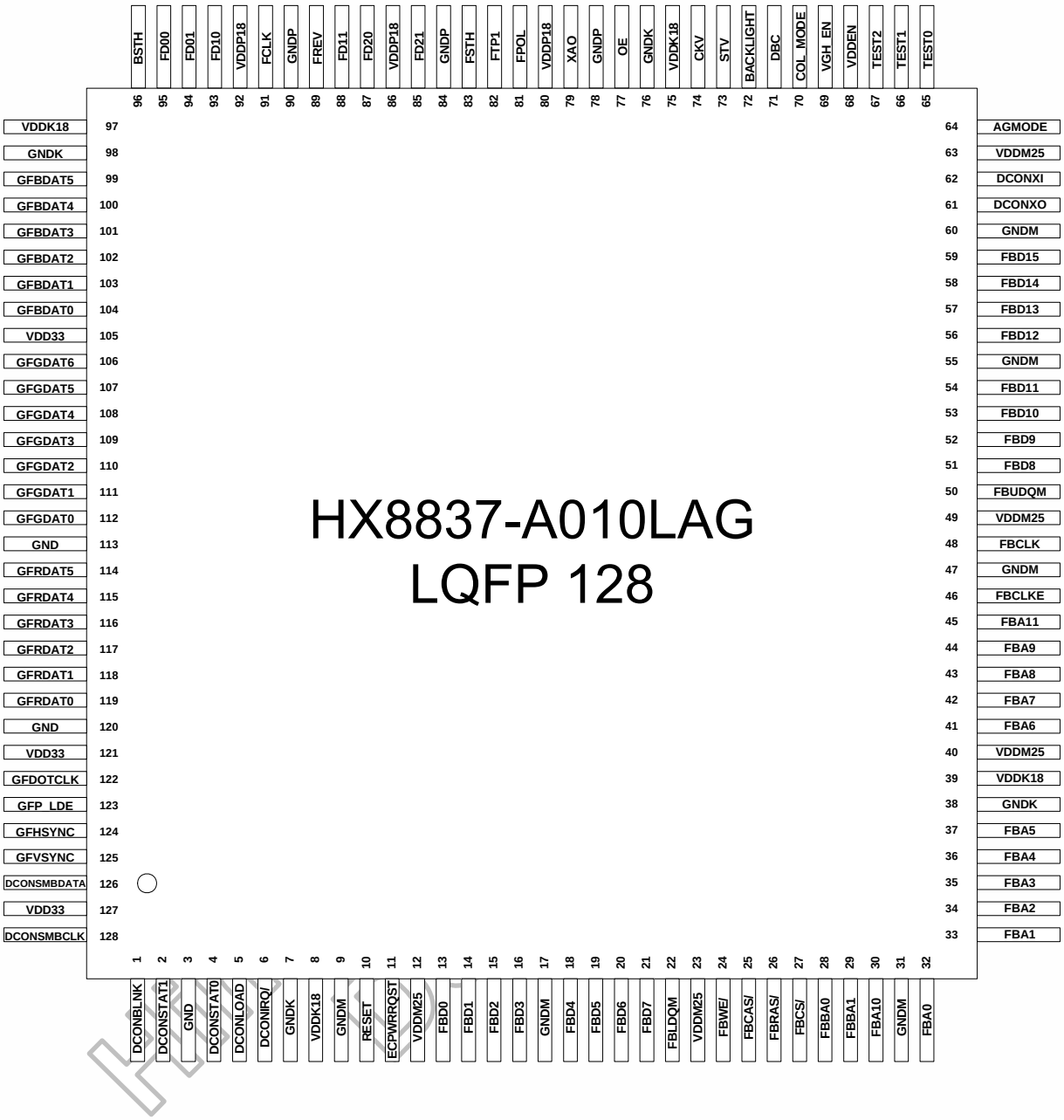
2. Features

- Autonomous display refresh, independent of the CPU or display controller's power state
- Support "color swizzling" to enable the OLPC TFT display to appear as a conventional 24-bit color panel
- Optional anti-aliasing improves text display in color mode
- Monochrome mode provides for a pixel-addressable automatic color->gray scale conversion mode
- Completely transparent to incoming video in "pass-through" mode, thereby emulating a simple LCD timing controller chip
- Automatic "flyby" mode prevents unnecessary writing to the attached SDRAM display buffer, and minimizes total power consumption
- Self-test capability supports efficient production line testing
- 128-pin LQFP package

3. Block Diagram



4. Pin Assignment



5. Pin Description

Pin Name	Pin No.	I/O	Description
Display interface pin			
GFBDAT5	99	In	Digital blue data 5 input
GFBDAT4	100	In	Digital blue data 4 input
GFBDAT3	101	In	Digital blue data 3 input
GFBDAT2	102	In	Digital blue data 2 input
GFBDAT1	103	In	Digital blue data 1 input
GFBDAT0	104	In	Digital blue data 0 input
GFGDAT6	106	In	Digital green data 6 input
GFGDAT5	107	In	Digital green data 5 input
GFGDAT4	108	In	Digital green data 4 input
GFGDAT3	109	In	Digital green data 3 input
GFGDAT2	110	In	Digital green data 2 input
GFGDAT1	111	In	Digital green data 1 input
GFGDAT0	112	In	Digital green data 0 input
GFRDAT5	114	In	Digital red data 5 input
GFRDAT4	115	In	Digital red data 4 input
GFRDAT3	116	In	Digital red data 3 input
GFRDAT2	117	In	Digital red data 2 input
GFRDAT1	118	In	Digital red data 1 input
GFRDAT0	119	In	Digital red data 0 input
GFDOTCLK	122	In	Pixel clock input (57MHz±1MHz)
GFP_LDE	123	In	Digital data enable input
GFHSYNC	124	In	Horizontal sync input
GFVSYNC	125	In	Vertical sync input
System interface pin			
DCONSMBCLK	128	In	Register I/O SMBUS clock
DCONSMDATA	126	In/Out	Register I/O SMBUS data
DCONBLNK	1	Out	DCON blanking status
DCONSTAT1	2	Out	DCON display active status 1
DCONSTAT0	4	Out	DCON display active status 0
DCONLOAD	5	In	DCON display load command request
DCONIRQ/	6	Out	DCON interrupt output
ECPWRRQST	11	In	EC power on request
SDRAM interface pin			
FBD0	13	In/Out	SDRAM data bit 0
FBD1	14	In/Out	SDRAM data bit 1
FBD2	15	In/Out	SDRAM data bit 2
FBD3	16	In/Out	SDRAM data bit 3
FBD4	18	In/Out	SDRAM data bit 4
FBD5	19	In/Out	SDRAM data bit 5
FBD6	20	In/Out	SDRAM data bit 6
FBD7	21	In/Out	SDRAM data bit 7
FBD8	51	In/Out	SDRAM data bit 8
FBD9	52	In/Out	SDRAM data bit 9
FBD10	53	In/Out	SDRAM data bit 10
FBD11	54	In/Out	SDRAM data bit 11
FBD12	56	In/Out	SDRAM data bit 12
FBD13	57	In/Out	SDRAM data bit 13
FBD14	58	In/Out	SDRAM data bit 14
FBD15	59	In/Out	SDRAM data bit 15
FBDA0	32	Out	SDRAM address bit 0
FBDA1	33	Out	SDRAM address bit 1
FBDA2	34	Out	SDRAM address bit 2
FBDA3	35	Out	SDRAM address bit 3

Pin Name	Pin No.	I/O	Description
FBDA4	36	Out	SDRAM address bit 4
FBDA5	37	Out	SDRAM address bit 5
FBDA6	41	Out	SDRAM address bit 6
FBDA7	42	Out	SDRAM address bit 7
FBDA8	43	Out	SDRAM address bit 8
FBDA9	44	Out	SDRAM address bit 9
FBDA10	30	Out	SDRAM address bit 10
FBDA11	45	Out	SDRAM address bit 11
FBWE/	24	Out	SDRAM write enable (Active low)
FBCAS/	25	Out	SDRAM column address select (Active low)
FBRAS/	26	Out	SDRAM row address select (Active low)
FBCS/	27	Out	SDRAM chip select (Active low)
FBBA0	28	Out	SDRAM bank select bit 0
FBBA1	29	Out	SDRAM bank select bit 1
FBLDQM	22	Out	SDRAM data mask bit 0
FBUDQM	50	Out	SDRAM data mask bit 1
FBCLKE	46	Out	SDRAM clock enable (Active high)
FBCLK	48	Out	SDRAM clock
DETTL/panel interface pin			
FD00	95	Out	DETTL data 00 to source driver
FD01	94	Out	DETTL data 01 to source driver
FD10	93	Out	DETTL data 10 to source driver
FD11	88	Out	DETTL data 11 to source driver
FD20	87	Out	DETTL data 20 to source driver
FD21	85	Out	DETTL data 21 to source driver
FCLK	91	Out	DETTL source driver clock
FSTH	83	Out	Front DETTL source driver start pulse
BSTH	96	Out	Back DETTL source driver start pulse
FTP1	82	Out	DETTL source driver TP pulse
FPOL	81	Out	DETTL source driver polarity pulse
FREV	89	Out	DETTL data inversion flag to source driver
STV	73	Out	Gate driver start pulse
CKV	74	Out	Gate driver clock
OE	77	Out	Gate driver output enable
VGH_EN	69	Out	LCD gate-high power enable
VDDEN	68	Out	LCD VDD enable
DBC	71	Out	LCD back light PWM control
BACKLIGHT	72	Out	LCD back light enable (Active high)
COL_MODE	70	Out	Color / Monochrome panel select
XAO	79	Out	Panel all gate initial control
Miscellaneous control			
RESET	10	In	DCON hardware reset input (Active low).
DCONXO	61	Out	Crystal output
DCONXI	62	In	Crystal input (14.318Mhz)
AGMODE	64	In	Self test mode enable pin (Active high)
TEST0	65	In	Test mode control pin 1 (Normal set low)
TEST1	66	In	Test mode control pin 1 (Normal set low)
TEST2	67	In	Test mode control pin 2 (Normal set low)
Power supply			
VDDP18	80,86,92	In	DETTL I/O pad power (1.8V)
GNDP	78,84,90	In	DETTL I/O pad ground
VDDM25	12, 23, 40, 49, 63	In	SDRAM I/O pad power (2.5V)
GNDM	9, 17, 31, 47, 55, 60	In	SDRAM I/O pad ground
VDD33	105, 121,	In	Digital I/O pad power (3.3V)

Pin Name	Pin No.	I/O	Description
	127		
GND	3, 113, 120	In	Digital I/O pad ground
VDDK18	8, 39, 75, 97	In	Core power (1.8V)
GNDK	7, 38, 76, 98	In	Core ground

6. Function Description

6.1 Color Swizzling

The first pixel of the first scan line is red, the second pixel of this scan line is green, and the third pixel is blue. This pattern repeats across the scan line. Note, however, that each subsequent scan line is offset from the prior scan line by one color component. The second scan line's first pixel is therefore green, its second pixel is blue, and its third pixel is red – this pattern is repeated across the second scan line. The third scan line's first pixel is blue, its second pixel is red, and its third pixel is green – this pattern is repeated across the third scan line. The patterns described above for the first three scan lines are then repeated in groups of three scan lines throughout the entire display panel.

6.2 Color Anti-Aliasing

Color Anti-Aliasing combines the current pixel's color value (at pixel coordinate V, H) with the matching color fields from the pixels that are above (V-1, H), below (V+1, H), to the left (V, H-1), and to the right (V, H+1) of the current pixel. It works by summing the values of the matching color field from these four neighboring pixels, shifting the result right 3 bits, and adding it to the current pixel's value shifted right by one bit.

$$Sb\_Pxl(x',y') = \{[Sb\_Pxl(x,y-1) + Sb\_Pxl(x+1,y) + Sb\_Pxl(x,y+1) + Sb\_Pxl(x-1,y)] >> 3 + [Sb\_Pxl(x,y) >> 1]\}$$

6.3 Monochrome Luminance

Monochrome Luminance is 19-bit input color values (again, in 6-7-6 RGB format) which are converted into 6-bit pixel display values via the following simple integer approximation to the standard NTSC luminance conversion formula:

$$Pixel\ Value = (R >> 2) + (R >> 4) + (G >> 1) + (G >> 4) + (B >> 3)$$

6.4 VGA Mode

The VGA mode is the DCON normal display mode. The DCON would display the CPU data.

6.5 DCON Mode

Automatic "flyby" mode prevents unnecessary writing to the attached SDRAM display buffer, and minimizes total power consumption

6.6 Self-Test Mode

At power-up the DCON samples the AGMODE pin to determine if it should enter normal operation (AGMODE Low), or self-test operation (AGMODE High). When the DCON is placed into self-test mode, and no input video clock is detected, the DCON will automatically cycle its display outputs through the sequence of (White, Black, Red, Green, Blue) every two seconds.

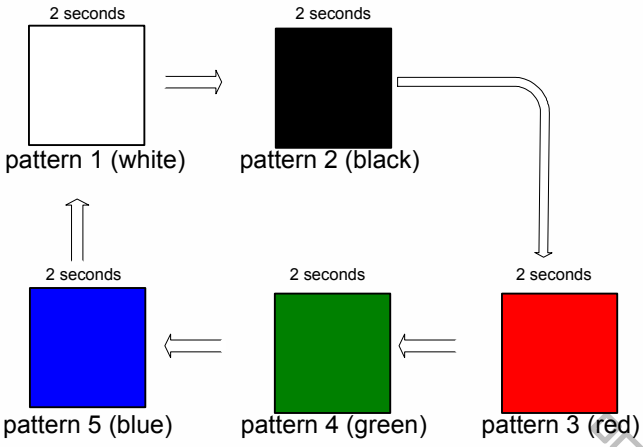


Figure 6. 1 Self-Test Mode Display Output Pattern

6.7 Debug Mode

In the Debug mode, two actions will occur. The LCD panel interface changes to support a conventional color LCD with red and green color sub-pixels.

6.8 Frame Buffer Organization

The 512Kx16 SDRAM frame buffer contains 1,048,576 bytes, yet the 1200x900 OLPC TFT panel contains 1,080,000 pixels.

6.9 Gate/Source Control Timing

This block generates control signals for source and gate drivers. The parameters of these signals are provided by registers of DCON. Detailed timing specifications are shown below.

Description	Symbol	1200x900	Unit
FSTH leading to DE leading	td1	2	FCLK
High duration of FSTH	td2	1	FCLK
FSTH leading to BSTH	td3	300	FCLK
FSTH leading to FTP1	td4	604	FCLK
High duration of FTP1	tw1	19	FCLK
FSTH leading to FPOL	td5	300	FCLK
High/Low duration of FPOL	tw2	1256(1)	FCLK
FSTH leading to CKV	td6	599	FCLK
High duration of CKV	tw3	307	FCLK
FSTH leading to STV	td7	302	FCLK
High duration of STV	tw4	628(1)	FCLK
FSTH leading to OE	td8	541	FCLK
High duration of OE	tw5	120	FCLK

Note: (1) The H-Total=1256 pixel, tw2 and tw4 are depend on the H-Total.

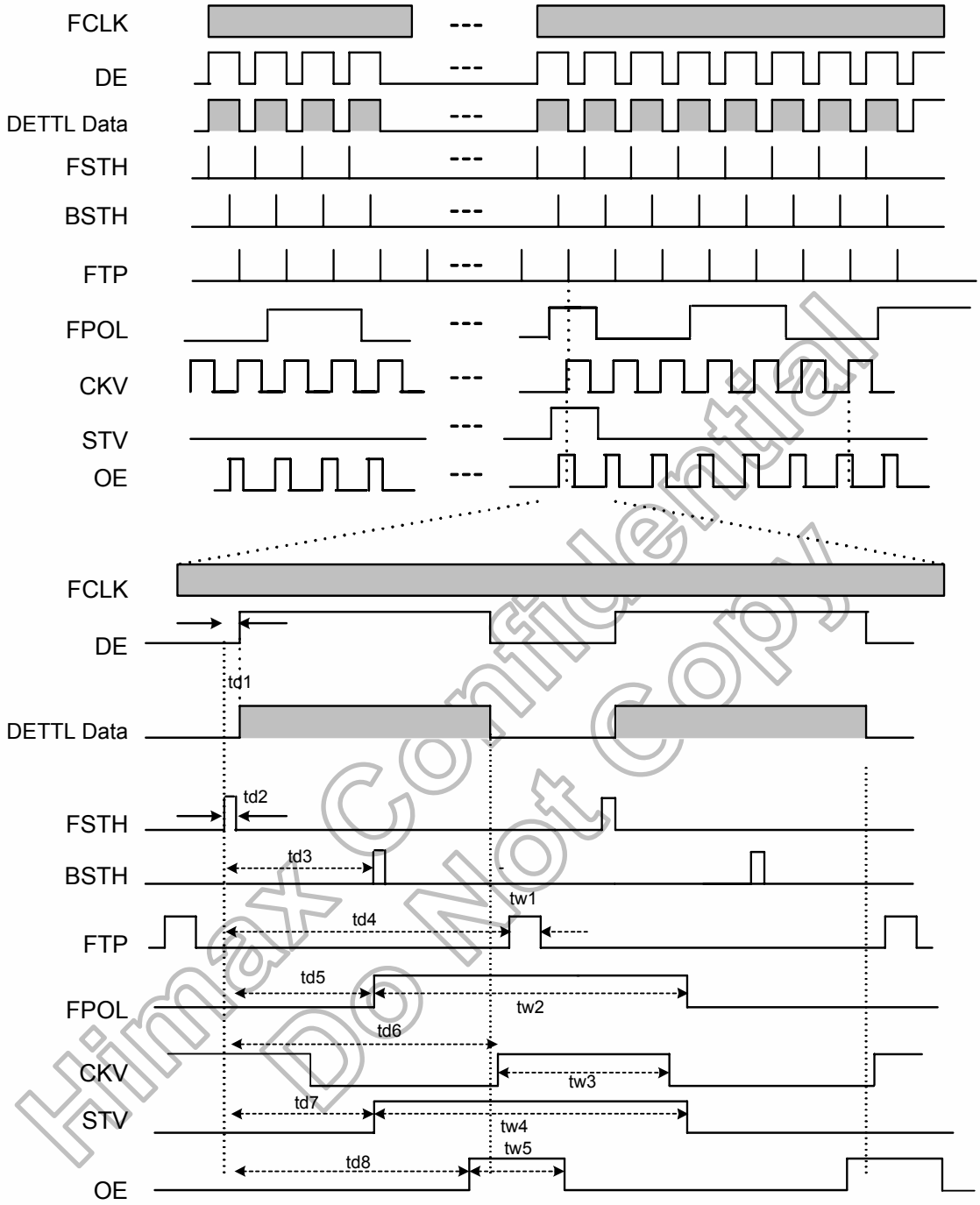


Figure 6. 2 Control Signal Output Timing Characteristics

6.10 POL inversion

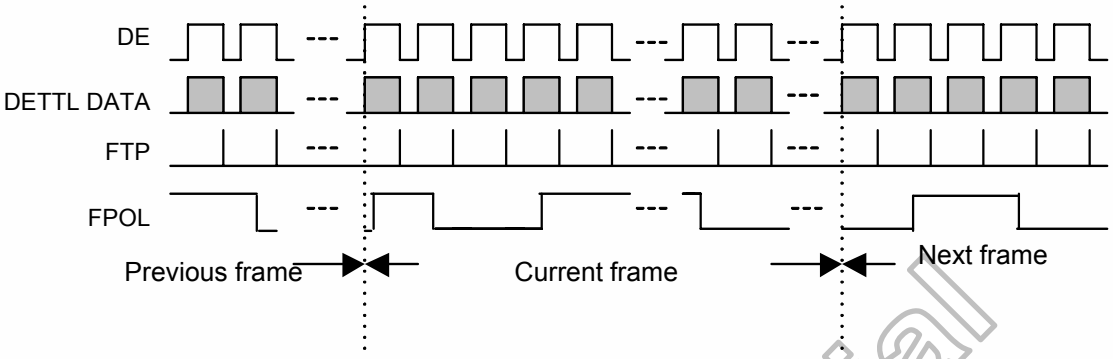


Figure 6. 3 POL 1+2 Line Frame Inversion

6.11 Input Signal Timing

Item	Symbol	Condition	1200x900	Unit
Horizontal total timing	HT	Typ.	1256	Clocks
Horizontal active timing	HVD	Typ.	1200	Clocks
Horizontal blank timing	DE_HB	Min.	40	Clocks
	DE_HB	Max.	600	Clocks
Vertical total timing	VT	Typ.	912	Lines
Vertical active timing	VVD	Typ.	900	Lines
Vertical blank timing	DE_VB	Min.	10(1)	Lines
	DE_VB	Max.	450(1)	Lines

Note: (1) VFP should be over 1 lines.

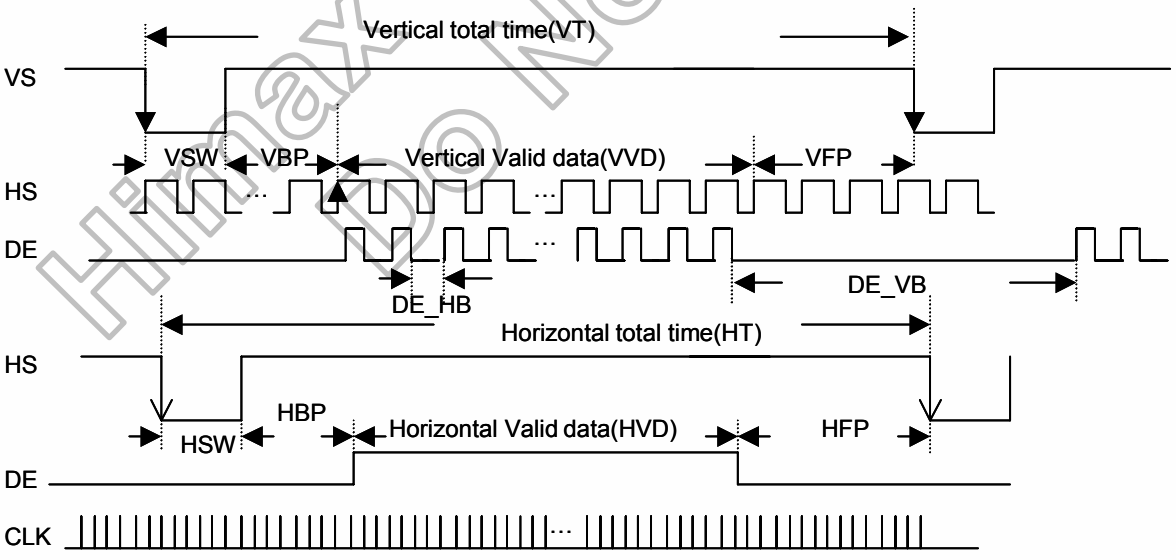


Figure 6. 4 Video Signal Format

6.12 Backlight Brightness

The Backlight Brightness is set by the Backlight Brightness register (8-bit). Only the upper 4 bits of this register are used – the lower 12 bits are undefined, and must be ignored. The Backlight Brightness register is used to set the duty cycle for the *DBC* output pin. A value of 00H corresponds to a duty cycle of 0% (fully off), while a value of 0FH corresponds to a duty cycle of 100%. Interim values may be used to set specific brightness levels.

6.13 DCON Register Definitions

The primary programming interface to the DCON chip is a 100 KHz serial SMBUS interface which allows read and write access to the chip's internal configuration registers. These registers are all 16-bit in length, and access is only supported as 16-bit registers

Register 00h：DCON ID+Revision

This 16-bit register is a read/only register which returns the DCON ASIC identifier, and revision number. The first pass of this silicon should return a hexadecimal value of 'DC01'H, the next revision should return 'DC02'H, etc.

Register 01h：DCON Display Mode

Bit 0： Pass-Through Disable

This bit controls whether the DCON will perform any manipulation of the input video. At power-up, this bit is automatically initialized to 0 by the DCON hardware, which causes the video outputs to directly follow the video inputs, and the DCON runs in Pass-Through mode.

Bit 1：DCON Sleep Mode

One key to the power efficiency of the DCON is its ability to enter a low power state in which the LCD is completely turned off, and the local SDRAM frame buffer is set to self-refresh mode – this mode is known as DCON Sleep Mode (or just Sleep mode). Under normal circumstances, the DCON will automatically enter Sleep mode as a result of prolonged system inactivity.

Bit 2：Auto Sleep Mode

The DCON will automatically stop the display process after *Display Timeout Value* video frames are outputted without system activity. Any time *DCONLOAD* is high, or when an incoming ECPWRRQST occurs, the internal display timeout register is automatically reset to the value in the *Display Timeout Value* register.

Bit 3：Backlight Enable

Backlight enable is used to determine whether the LCD's backlight should be turned on while the display is enabled – set this to 1 to turn on the backlight.

Bit 4：Video Blanking

Video blanking is used to display "black" on the screen, without affecting the contents of the DCON's frame buffer, or the power state of the LCD.

Bit 5：Color Swizzling Enable

This bit enables the DCON color swizzing function.

Bit 6：Color Anti-Aliasing Enable

This bit enables the DCON Color Anti-Aliasing function.

Bit 7：Monochrome Luminance Enable

This bit enables the DCON Monochrome Luminance function.

Bit 8：ScanLine Interrupt Enable

Setting this bit to 1 enables the DCON's ScanLine Interrupt output to be generated during the video scan line which is programmed into the *ScanLine Interrupt Value* register.

Bit 9-11：DotClock Divider

In order to support minimum power drain, the DCON supports the ability to reduce the frequency of the panel interface *DotClock*. The DotClock divider alone will result in actual panel refresh rates of 50.00 Hz, 25.00 Hz, 16.67 Hz, 12.50 Hz, 10.00 Hz, 8.33 Hz, 7.14 Hz, or 6.25 Hz

Bit 12-13：Reserved

These register bits are reserved.

Bit 14：Debug Mode Enable

This bit enables the DCON Debug Mode function.

Bit 15：Self-Test Mode

This bit enables the DCON Self-Test function.

Register 02h：Horizontal Resolution

This 16-bit register contains the number of displayed pixels per horizontal scan line. This is normally 1200.

Register 03h：Horizontal Total

This 16-bit register contains the total number of dot clocks per horizontal scan line.

Register 04h：Horizontal Sync Start & Width

This 16-bit register contains two 8-bit registers. The most-significant byte of the register contains the horizontal sync start register. After “Horizontal Resolution” dot clocks occur on each line, HSync will be generated after “HSync Start” additional clocks occur. The least-significant byte of this register contains the number of clocks that HSync will remain active, once HSync is generated.

Register 05h：Vertical Resolution

This 16-bit register contains the total number of scan lines to be displayed per video frame. This will normally contain the value 900.

Register 06h：Vertical Total

This 16-bit register contains the total number of scan line durations that will occur per video frame. For clarity, the TFT panel refresh rate in Hz will equal:

*DotClock / (Horizontal Total * Vertical Total)*.

Register 07h：Vertical Sync Start & Width

This 16-bit register contains two 8-bit registers. The most significant byte of the register contains the vertical sync start register. After “Vertical Resolution” scan lines are displayed, VSync will be generated after “VSync Start” additional scan line times occur. The least-significant byte of this register contains the number of scan lines that VSync should remain active, once VSync is generated.

Register 08h：Display Timeout Value

In order to save power, the DCON automatically powers down the display outputs and enters *DCON Sleep Mode*. This register contains the number of output video frames before this automatic powerdown will occur.

Register 09h：ScanLine Interrupt Value

In order to properly synchronize the CPU’s video outputs with the DCON’s video outputs, the DCON contains the ability to allow system software to synchronize with the display process by generating a CPU interrupt at any given scan line of the display.

Register 0Ah：Backlight Brightness

Only the upper 4 bits of this register are used – the lower 12 bits are undefined, and must be ignored.

Register 41h：Memory Controller Setting

Bit 0： DLL Setting Load Enable

This bit enables the setting of DLL in order to modulate setup/hold time of memory.

Bit 8： Memory Controller Power-down Enable

This bit enables the memory controller power-down function.

Register 42h：Memory Controller Setting

Bit 0： Memory Initial

This bit is the memory controller soft reset.

Register 4Ch：TTL and DETTL I/O Driving Strength Setting

The registers set up the TTL and DETTL I/O driving strength.

Table 6-1: DCON Details

Sub AD	Name	R/W	Bits	Default	Description
00h	DCON ID + Revision	RO	15-0	DCXXh	DCON ID + Revision
01h	Pass-Through Disable	R/W	0	0	Pass through mode enable bit (0:enable 1:disable)
	DCON Sleep Mode	R/W	1	1	DCON sleep mode enable bit (0:disbale 1:enable)
	Auto Sleep Mode	R/W	2	0	DCON auto sleep enable bit (0:disbale 1:enable)
	Backlight Enable	R/W	3	0	Backlight enable bit (0:disbale 1:enable)
	Video Blanking	R/W	4	1	Output black data enable bit (0:disbale 1:enable)
	Color Swizzling Enable	R/W	5	0	Color swizzing enable bit (0:disbale 1:enable)
	Color Anti-Aliasing Enable	R/W	6	0	Color anti-aliasing enable bit (0:disbale 1:enable)
	Monochrome Luminance Enable	R/W	7	0	Monochrome luminance enable bit (0:disbale 1:enable)
	ScanLine Interrupt Enable	R/W	8	0	Scan line interrupt enable bit (0:disbale 1:enable)
	DotClock Divider	R/W	11-9	0	Output clock frequency setting bits INPUT_FORMAT [2:0] / Description Panel refresh rate 0h: 50.00 HZ 1h: 25.00 HZ 2h: 16.67 HZ 3h: 12.50 HZ 4h: 10.00 HZ 5h: 8.33 HZ 6h: 7.14 HZ 7h: 6.25 HZ
	Reserved	-	12	-	Reserved
	Reserved	-	13	-	Reserved
	Debug Mode Enable	R/W	14	0	Debug mode enable bit (0:enable 1:disable)
	Self-Test Mode	R/W	15	0	Self test mode enable bit (0:enable 1:disable)
02h	Horizontal Resolution	R/W	15-0	04B0h	Horizontol resolution
03h	Horizontal Total	R/W	15-0	04E8h	Horizontol total

Sub AD	Name	R/W	Bits	Default	Description
04h	Horizontal Sync Start & Width	R/W	15-0	1808h	most-significant byte of the register contains the horizontal sync start register least-significant byte of this register contains the number of clocks that HSync will remain active
05h	Vertical Resolution	R/W	15-0	0384h	Vertical Resolution
06h	Vertical Total	R/W	15-0	0390h	Vertical Total
07h	Vertical Sync Start & Width	R/W	15-0	0403h	most significant byte of the register contains the vertical sync start register least-significant byte of this register contains the number of scan lines that VSync should remain active
08h	Display Timeout Value	R/W	15-0	FFFFh	This register contains the number of output video frames before DCON automatic sleep
09h	ScanLine Interrupt Value	R/W	15-0	0000h	This register is written with the output video scan line number during which the interrupt should be generated
0Ah	Backlight Brightness	R/W	11-0	-	Reserved
		R/W	15-12	Fh	Brightness register is used to set the duty cycle for the DBC output pin **INPUT_FORMAT [3:0]** / **Description Duty** 0h / 0% (fully off) Fh / 100% (fully on)
0Bh | 40h	DCON Internal Setting	WO	-	-	DCON internal setting
41h	DLL Setting Load Enable	WO	0	1h	Load DLL setting for clock delay (o : disable 1: enable)
	Reserved		7-1	0h	Reserved
	Memory Controller Power down Enable		8	1h	Memory controller power down enable (o : disable 1: enable)
	Reserved		15-9	0h	Reserved
42h	Memory Initial	WO	0	1h	Memory controller software reset
	Reserved		15-1	0h	Reserved
43h | 4Bh	DCON Internal Setting	WO	-	-	DCON internal setting
4Ch	TTL Driving Strength	WO	2-0	0h	TTL signal driving strength select (111 : max ; 000 : min)
	TTL Slew Rate		3	0h	TTL signal slew Rate Control pin (0 : High SR ; 1 : Low SR)
	DETTL FSTH/BSTH Driving Strength		5-4	3h	STH signal driving strength select (11 : max ; 00 : min)
	DETTL Data Driving Strength		7-6	2h	DETTL data signal driving strength select (11 : max ; 00 : min)
	DETTL Clock Driving Strength		9-8	3h	DETTL clock signal driving strength select (11 : max ; 00 : min)
	DETTL Rev Driving Strength		11-10	2h	DETTL rev signal driving strength select (11 : max ; 00 : min)
	DETTL Source Control Driving Strength		13-12	1h	DETTL source driver control signal driving strength select (11 : max ; 00 : min)
	DETTL Gate Control Driving Strength		15-14	0h	DETTL gate driver control signal driving strength select (11 : max ; 00 : min)

Sub AD: Register sub address
Name: Register name
RO: Register read only
R/W: Register read/write direction
WO: Register write only
Bits: Register bit range
Default: Register Power on reset value

7. DC Characteristics

7.1 Absolute Maximum Rating

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply voltage	VDD	-0.5	-	4.6	V
CMOS/TTL input voltage	VIN	-0.5	-	VDD	V
CMOS/TTL output voltage	VOUT	-0.5	-	VDD	V
Storage temperature	T_{STG}	-40	-	125	℃
Junction temperature	T_I	-	125	-	℃
Thermal resistance (junction ambient)	Θ_{iA}	-	58.7	-	℃/W

7.2 Recommended Operating Conditions

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply Voltage	VDDP18	1.62	1.8	1.98	V
	VDDM25	2.25	2.5	2.75	V
	VDD33	3.0	3.3	3.6	V
	VDDK18	1.62	1.8	1.98	V
Operating Temperature	T_A	-10	25	85	℃

7.3 DC Electrical Characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Supply Current	I_{DD}	F=57MHz pixel checker pattern	-	T.B.D.	-	mA
3.3V CMOS/TTL DC Specifications						
High Level Input Voltage	V_{33IH}	-	1.67	-	VDD33	V
Low Level Input Voltage	V_{33IL}	-	VSS	-	0.77	V
High Level Output Voltage	V_{33OH}	-	2.97	-	VDD33	V
Low Level Output Voltage	V_{33OL}	-	VSS	-	0.33	V
Input Current	I_{33IN}	-	-1	-	1	μA
2.5V CMOS/TTL DC Specifications						
High Level Input Voltage	V_{25IH}	-	1.19	-	VDDM25	V
Low Level Input Voltage	V_{25IL}	-	VSS	-	0.62	V
High Level Output Voltage	V_{25OH}	-	2.25	-	VDDM25	V
Low Level Output Voltage	V_{25OL}	-	VSS	-	0.25	V
Input Current	I_{25IN}	-	-1	-	1	μA
1.8V CMOS/TTL DC Specifications						
High Level Input Voltage	V_{18IH}	-	1.01	-	VDDP18	V
Low Level Input Voltage	V_{18IL}		VSS	-	0.44	V
High Level Output Voltage	V_{18OH}		1.62	-	VDDP18	V
Low Level Output Voltage	V_{18OL}		VSS	-	0.18	V
Input Current	I_{18IN}	-	-1	-	1	μA

7.4 ESD Parameters

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Human Body Model	HBM	-	T.B.D.	-	V
Machine Model (C=200pF , R=0Ω)	MM	-	T.B.D.	-	V

8. AC Characteristics

8.1 Phase Lock Loop Wake-up Time

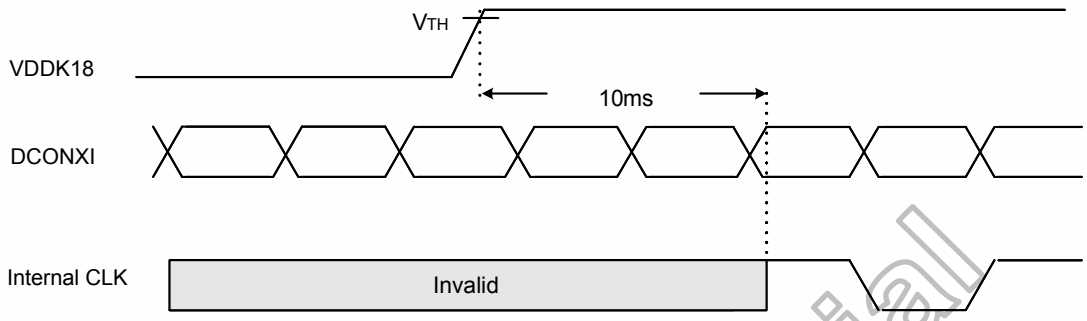


Figure 8. 1 PLL Wake-up Time

8.2 Power up Sequence

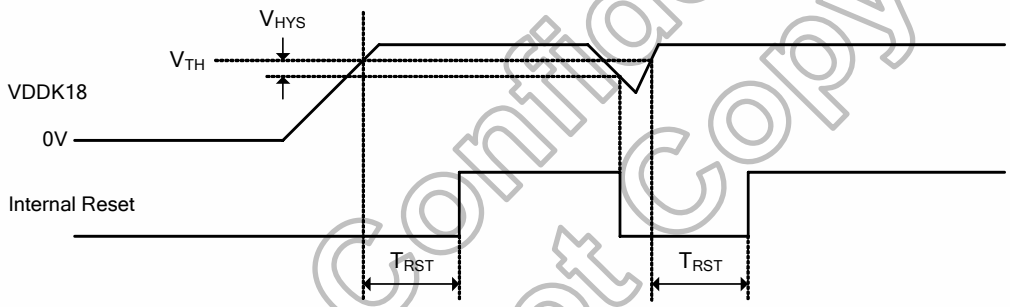


Figure 8. 2 Power up Sequence

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Reset threshold voltage	$V_{(TH)}$	-	T.B.D.	T.B.D.	T.B.D.	V
Hysteresis voltage	V_{HYS}	-	-	T.B.D.	-	mV
Reset duration	$t_{(RST)}$	R=1.5MΩ,C=0.1μF	-	T.B.D.	-	ms

8.3 SDRAM AC Electrical Characteristics

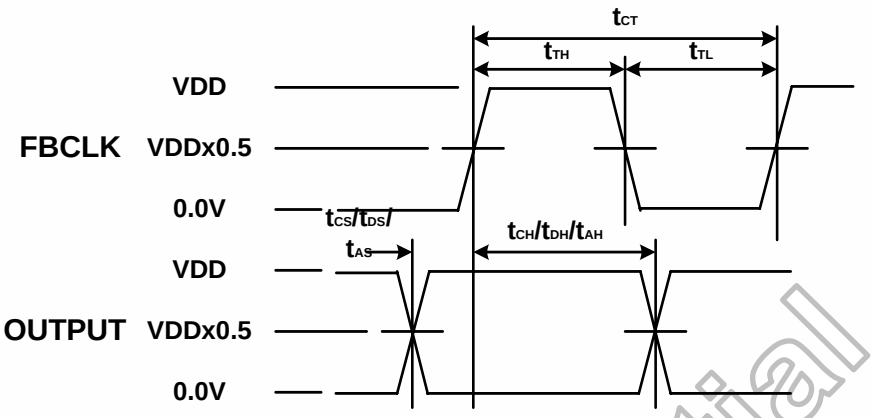


Figure 8. 3 SDRAM AC Characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Clock Cycle Time	T_{CT}	-	T.B.D.	T.B.D.	T.B.D.	ns
Clock high level width	T_{CH}	-	T.B.D.	T.B.D.	T.B.D.	ns
Clock low level width	T_{CL}	-	T.B.D.	T.B.D.	T.B.D.	ns
Command setup time(FBCS/, FBCAS/, FBRAS/)	T_{CS}	-	T.B.D.	T.B.D.	T.B.D.	ns
Command hold time(FBCS/, FBCAS/,FBRAS/)	T_{CH}	-	T.B.D.	T.B.D.	T.B.D.	ns
Output data setup time	T_{DS}	-	T.B.D.	T.B.D.	T.B.D.	ns
Output data hold time	T_{DH}	-	T.B.D.	T.B.D.	T.B.D.	ns
Address data setup time	T_{AS}	-	T.B.D.	T.B.D.	T.B.D.	ns
Address data hold time	T_{AH}	-	T.B.D.	T.B.D.	T.B.D.	ns

8.4 DETTL AC Electrical Characteristics

DETTL output data format

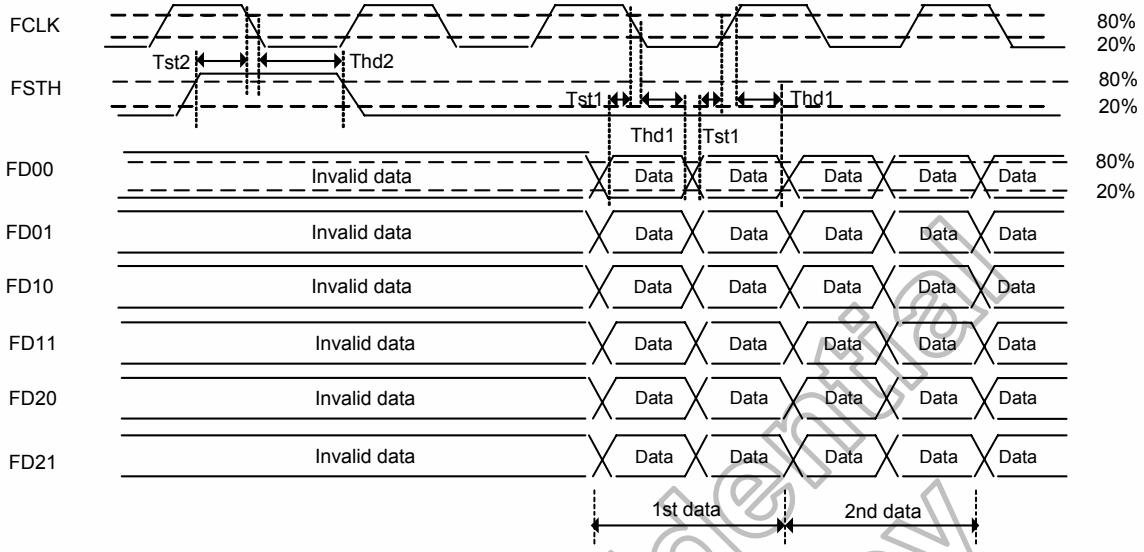
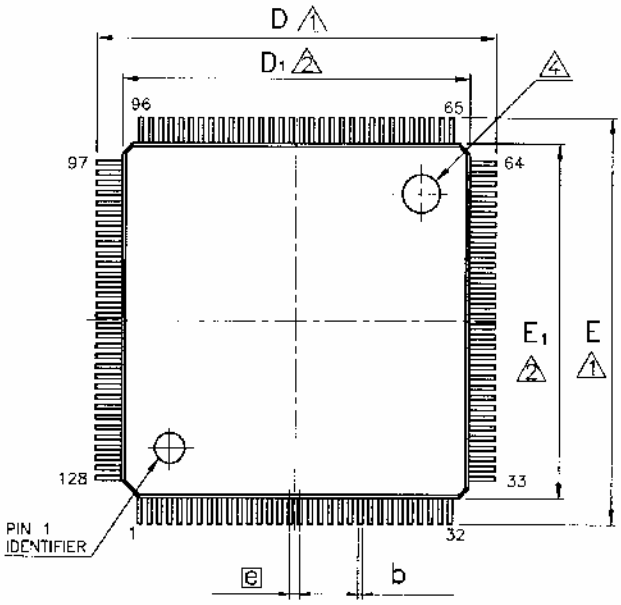


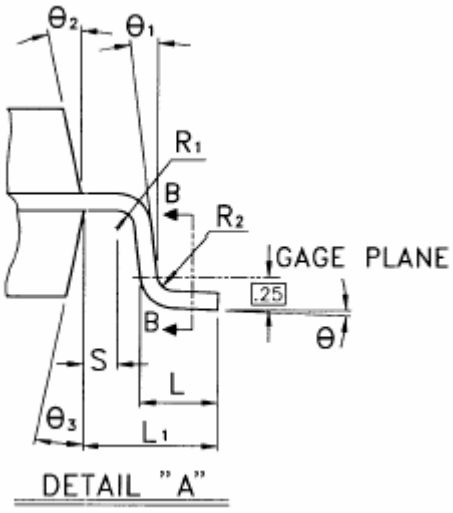
Figure 8. 4 DETTL Output Data Mapping

FCLK = 28.6MHz, Temp = 25℃

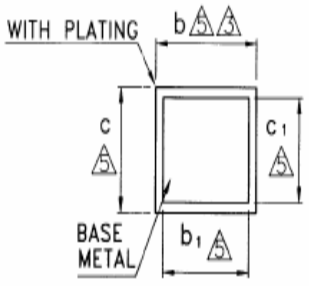
Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Data setup time	Tst1	-	-	T.B.D.	-	ns
Data hold time	Thd1	-	-	T.B.D.	-	ns
Horizontal Start pulse setup time	Tst2	-	-	T.B.D.	-	ns
Horizontal Start pulse hold time	Thd2	-	-	T.B.D.	-	ns

9. Package Outline Dimensions

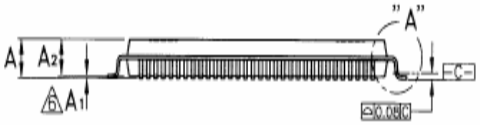




Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	12°TYP			12°TYP		
θ_3	12°TYP			12°TYP		

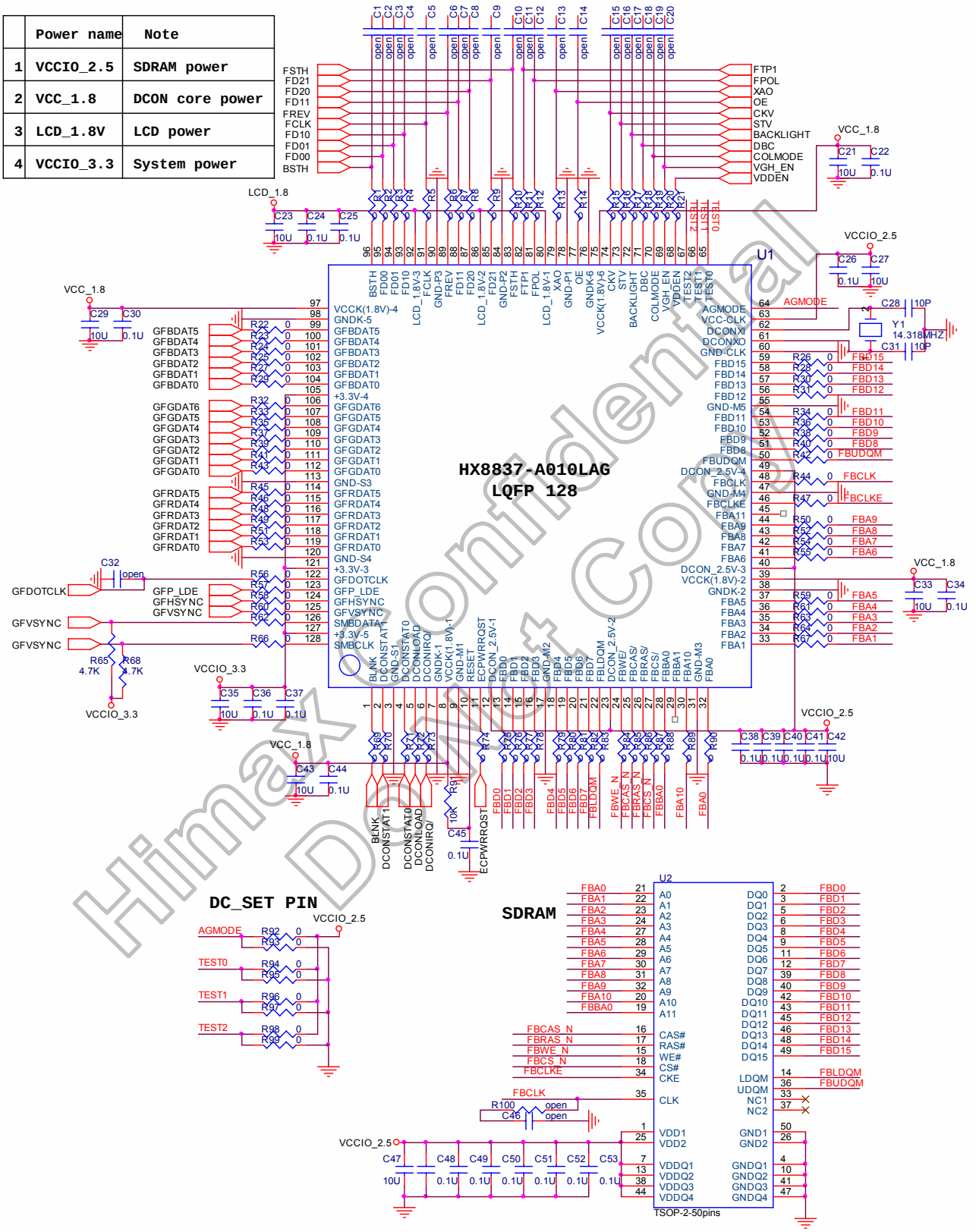


SECTION B-B



10. Reference Circuit

	Power name	Note
1	VCCIO_2.5	SDRAM power
2	VCC_1.8	DCON core power
3	LCD_1.8V	LCD power
4	VCCIO_3.3	System power



11. Ordering Information

Device	Package	Description
HX8837-A010LAGA-01A	128 pin LQFP Green package	First version(Register 0：DCON ID+Revision=DC01h)
HX8837-A010LAGC-01B	128 pin LQFP Green package	Register 0：DCON ID+Revision=DC02h

12. Revision History

Version	Date	Description of Changes
01	2007/03/27	New setup