

CL1B Block Diagram

K
2011-03-21

- VTERM(+0.9V)
- VTT(+1.05V)
- +1.5VSUS
- +1.5V
- +1.8VMEM
- +1.8V
- +2.5V
- 3VPCU
- +3.3V
- +3.3VSUS
- LCD_3.3V
- LCD_5V
- +5V

C7-M (ULV)

VCORE:+1.196 ~ +0.748
VCCP:+1.05V
VCCA:+1.8V or +1.5V

CPU VCORE

Clock Gengerator
ICS9UM7002

Frame Buffer

7" LCD

DCON

VX855(U)

VTT:VCCP (+1.05V)
VCC15:+1.5V or +1.2V
VCC33:+3.3V
VCCMEM:+1.8V
VSUS15:+1.5VSUS
VSUS33:+3.3VSUS

DDRII 1GB

MICRO SD

Camera

WLAN Conn.

WLAN Module

Card Reader
SD Card SLOT

Int. SPK

HDA CODEC
CX20582

HD Audio

Audio Jack

Int. Mic

USB PORT X3

EC
KB3700

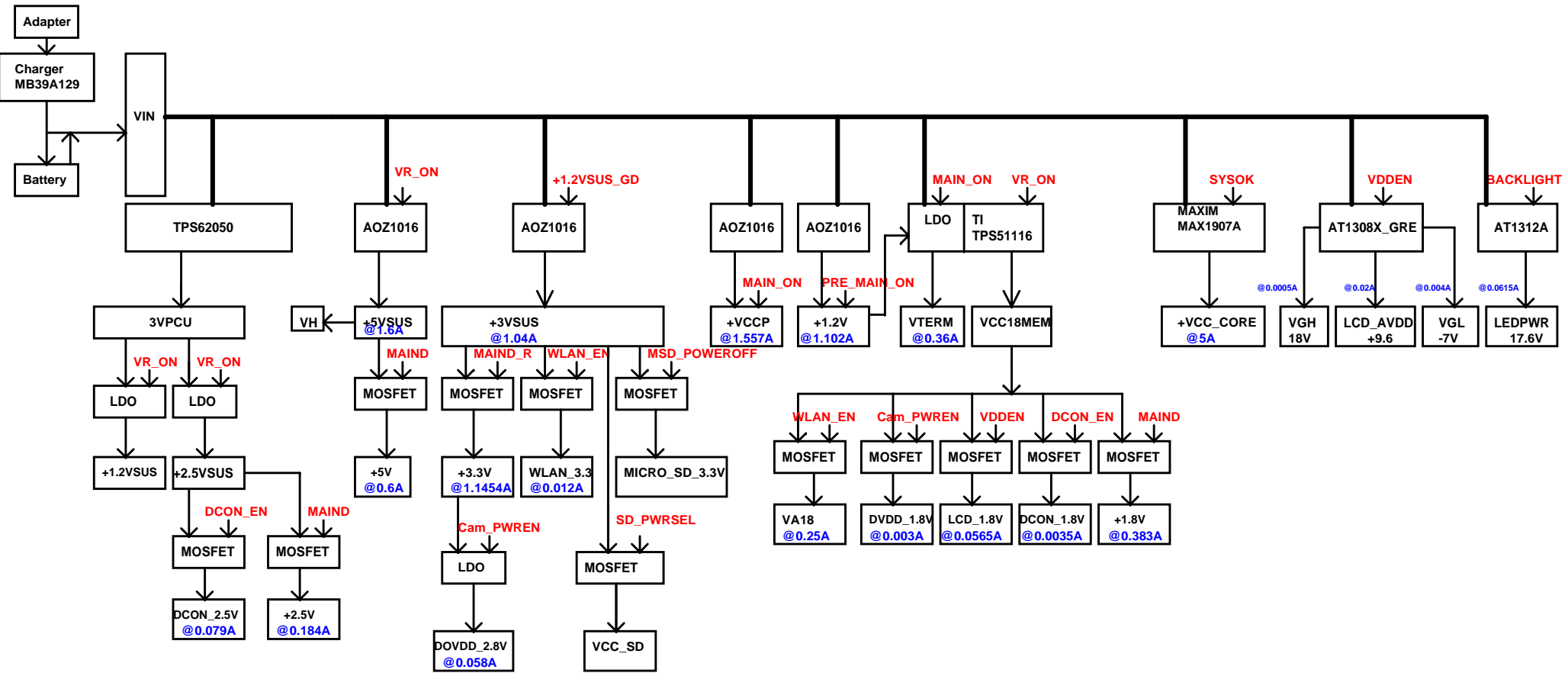
SPI Flash

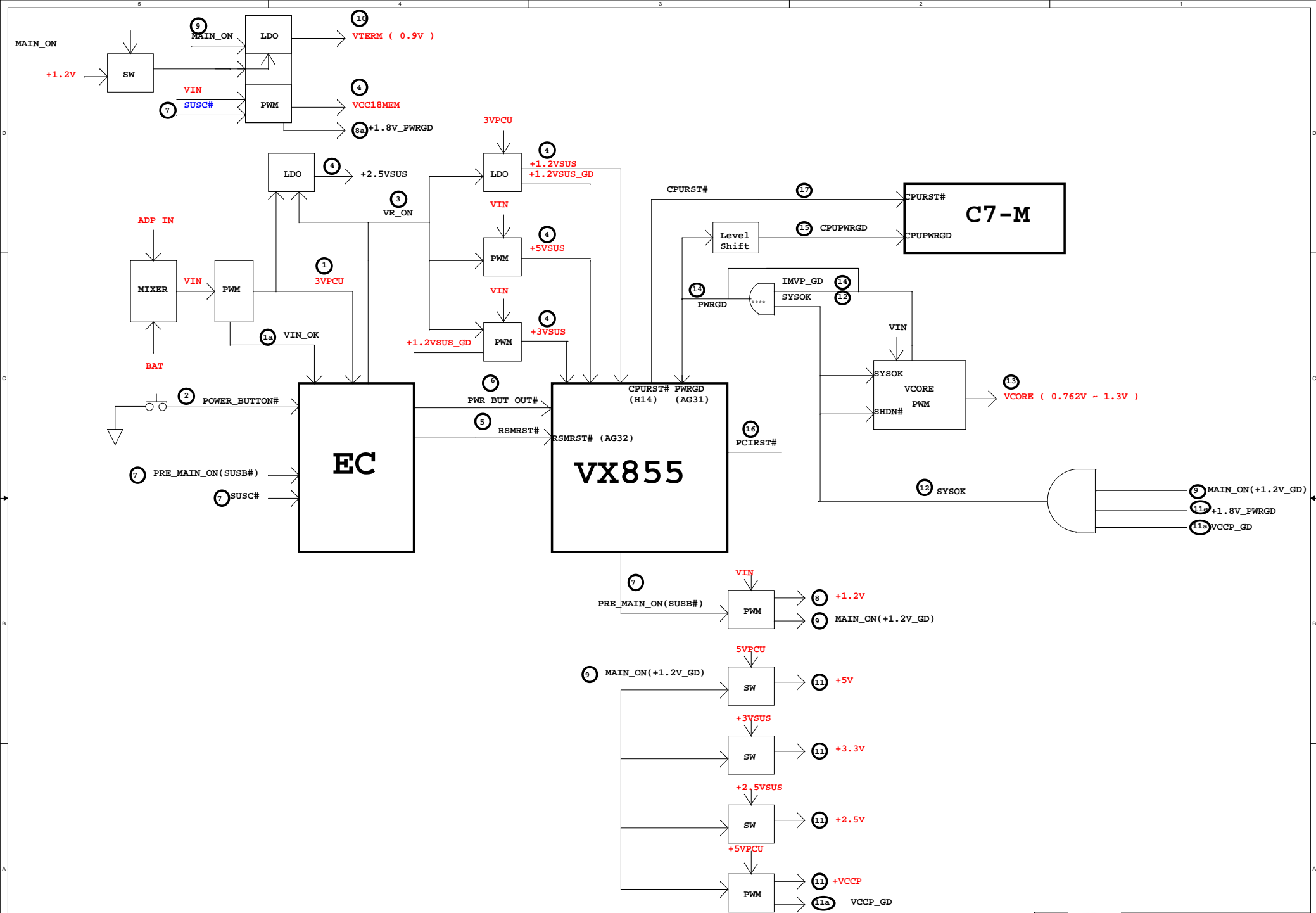
Int. KB

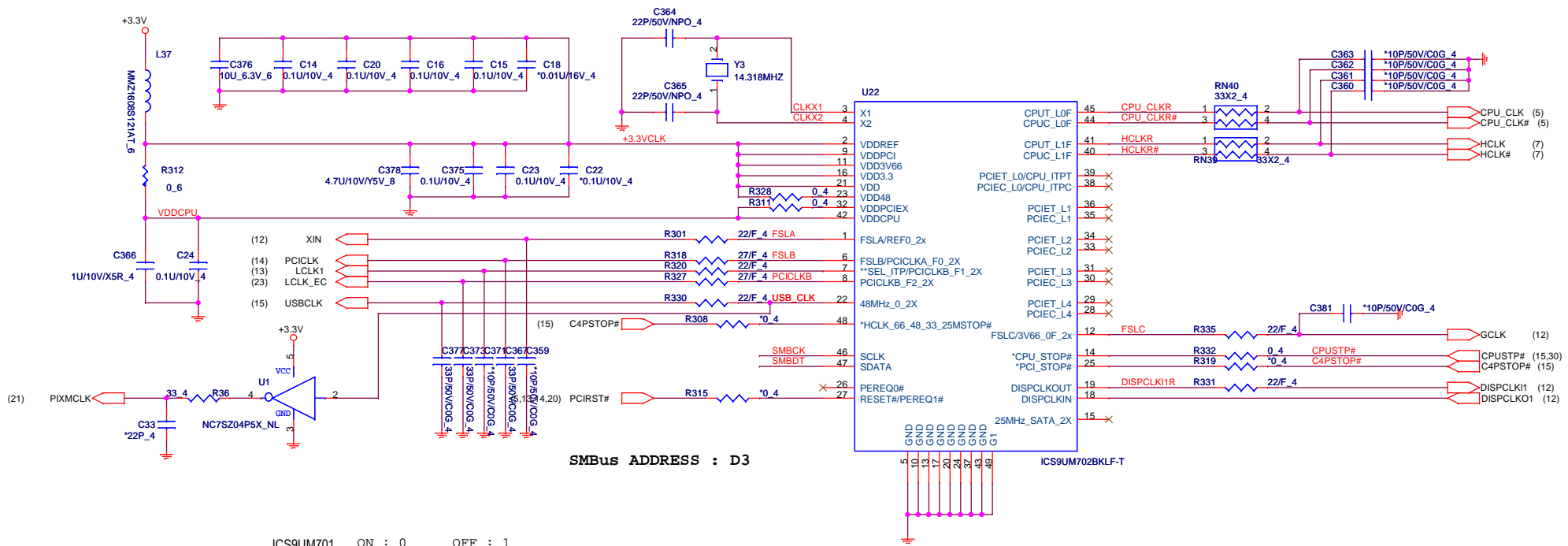
T/P

Battery

Charger



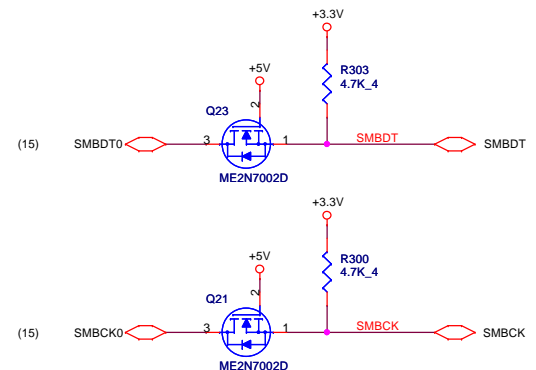
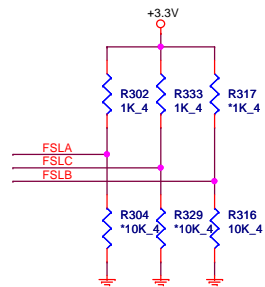


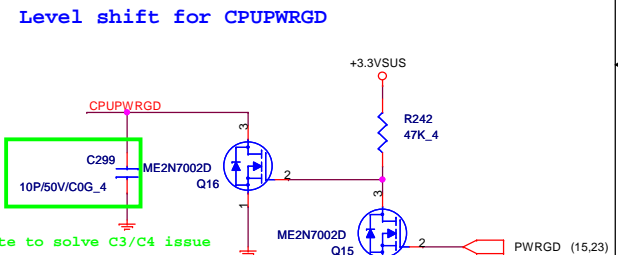
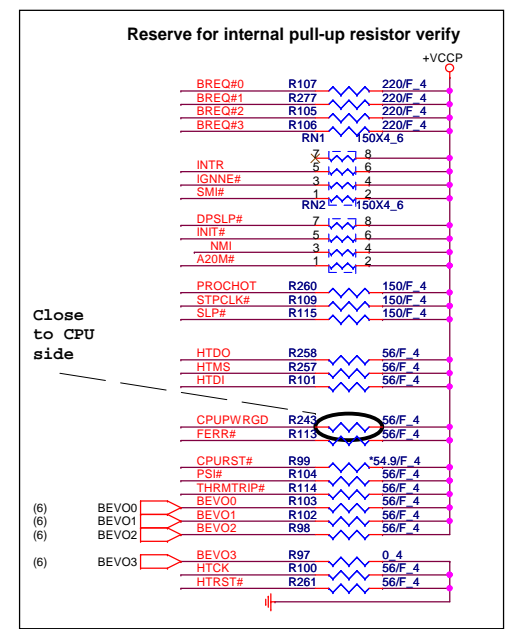
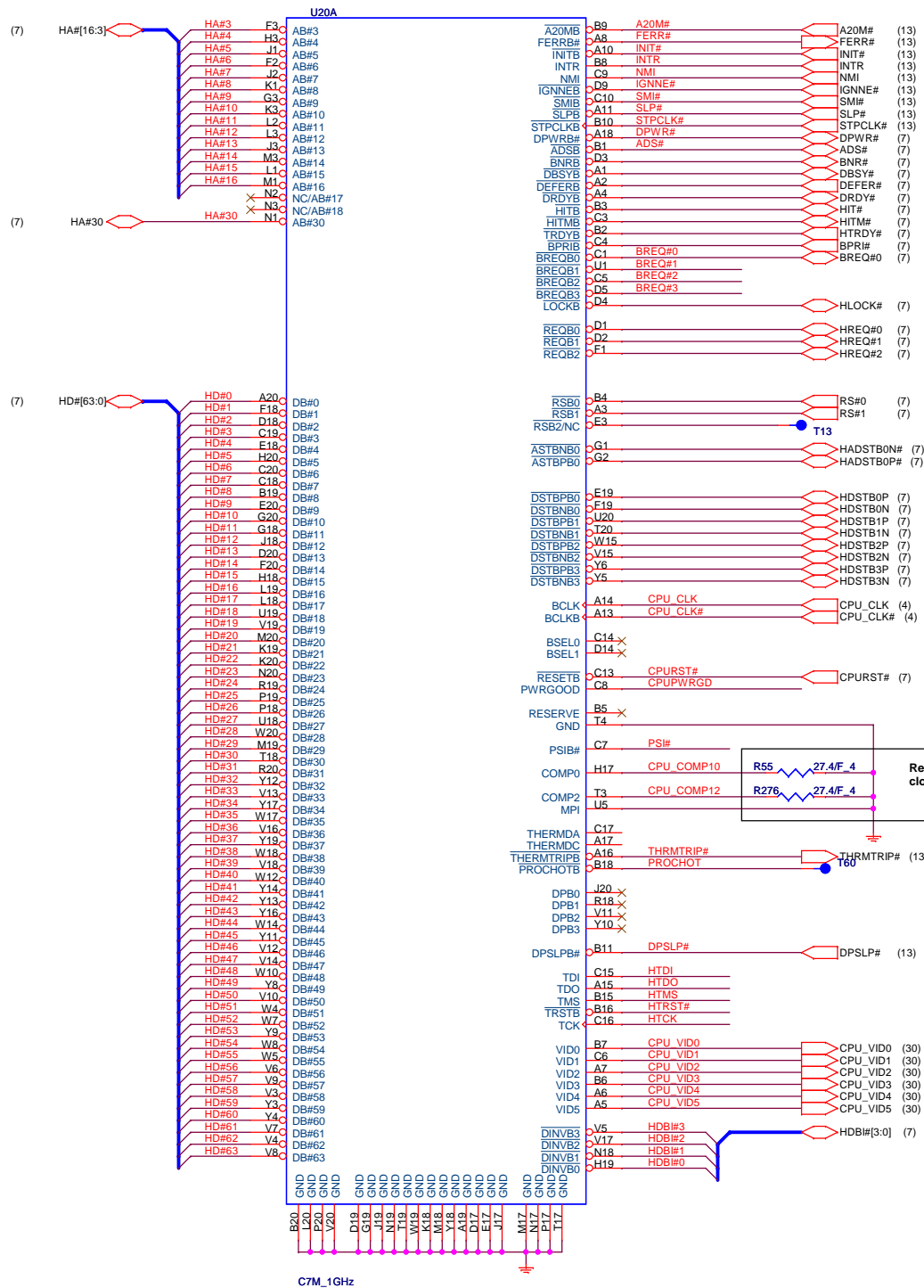


SMBus ADDRESS : D3

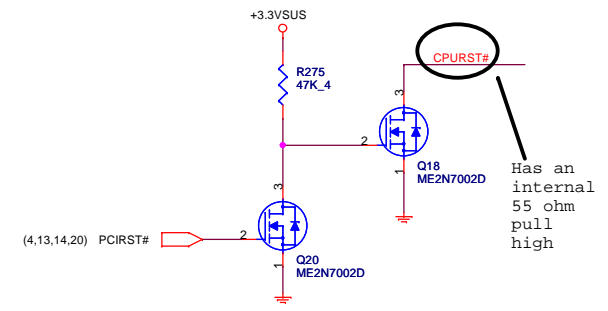
ICS9UM701 ON : 0 OFF : 1

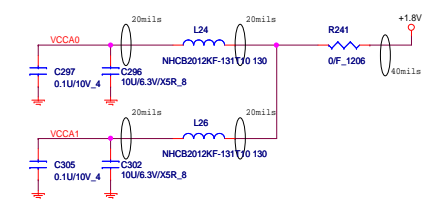
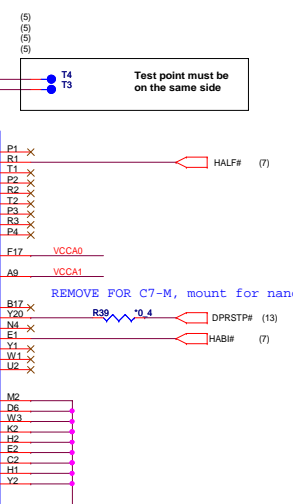
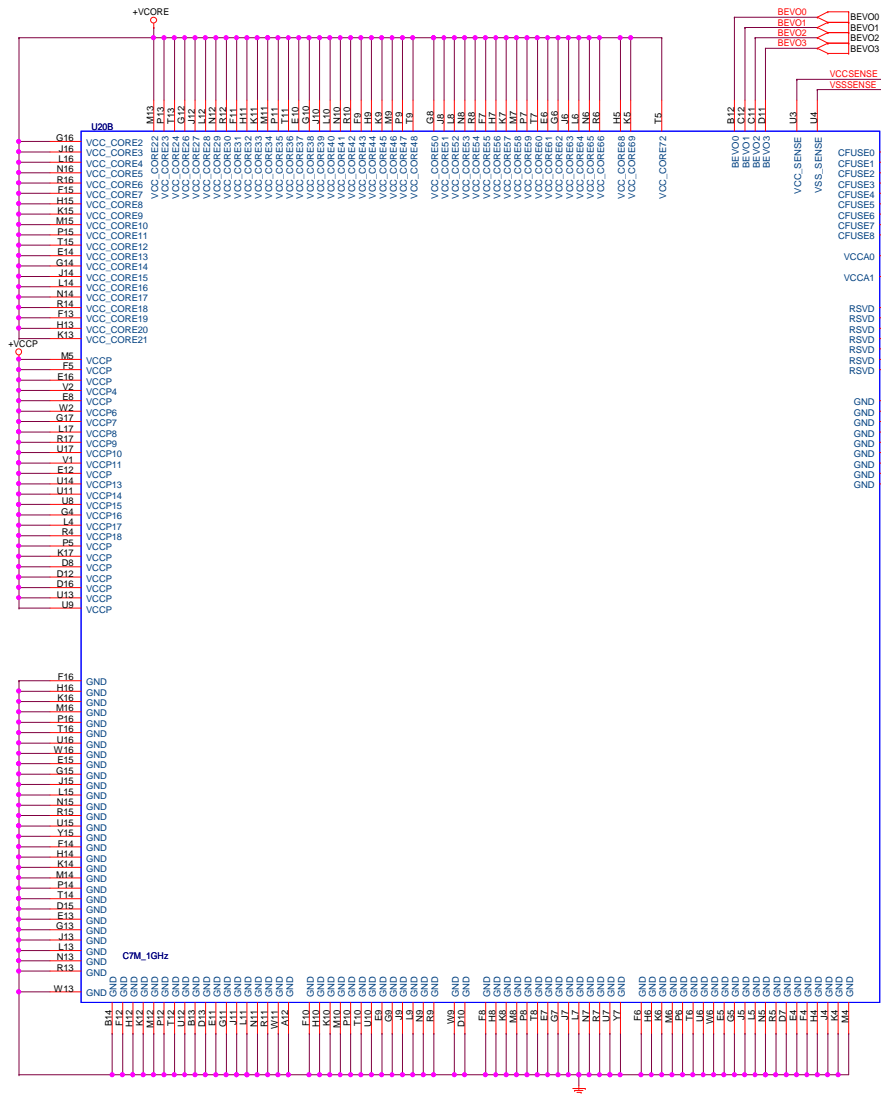
3	2	1	CPU	PCI
FSLA	FSLC	FSLB	CPU	PCI
0	0	0	266.66	33
1	0	0	133.33	33
0	0	1	200	33
1	0	1	166.66	33
0	1	0	333.33	33
1	1	0	100	33
0	1	1	400	33
1	1	1	200	33



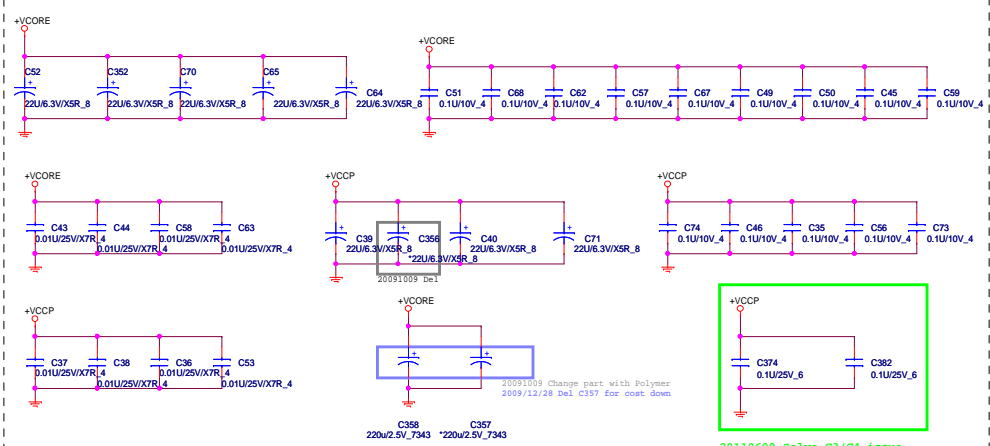


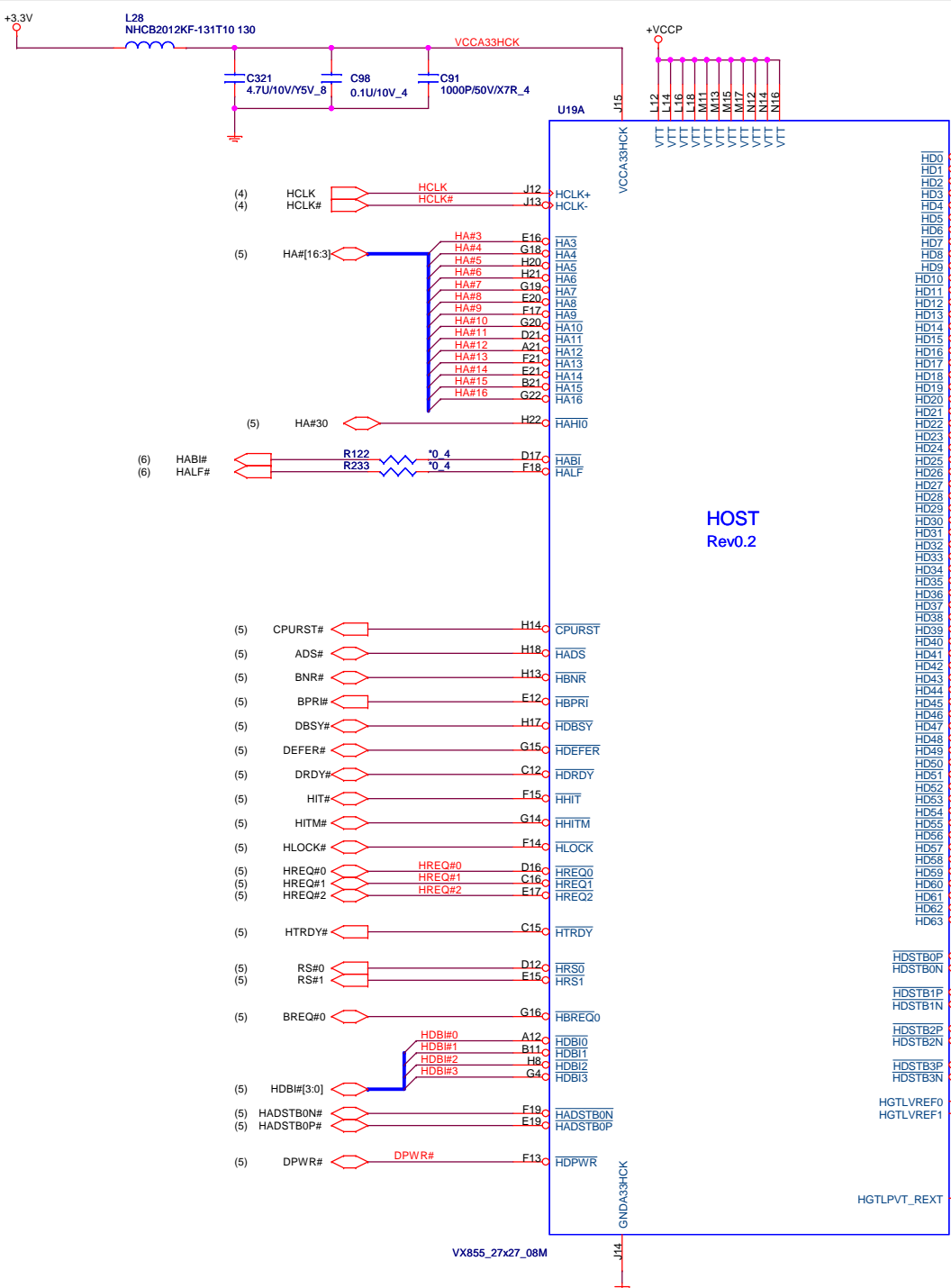
20110609 Populate to solve C3/C4 issue



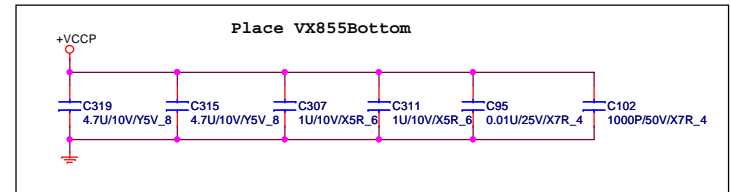


Put the caps. on the bottom of CPU.
Please refer to the placement below.

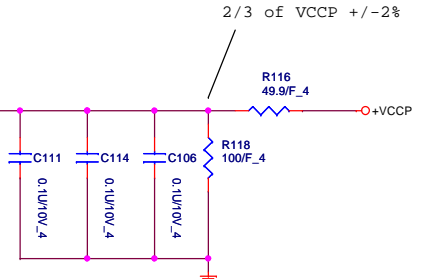
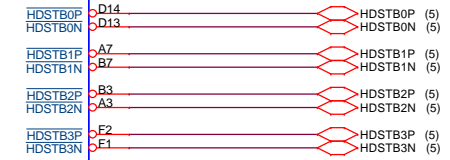


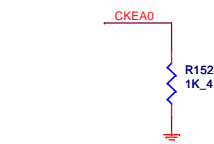
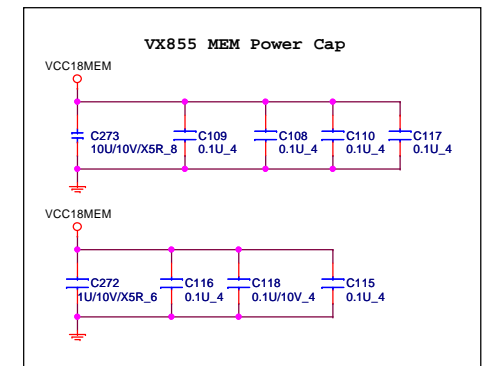
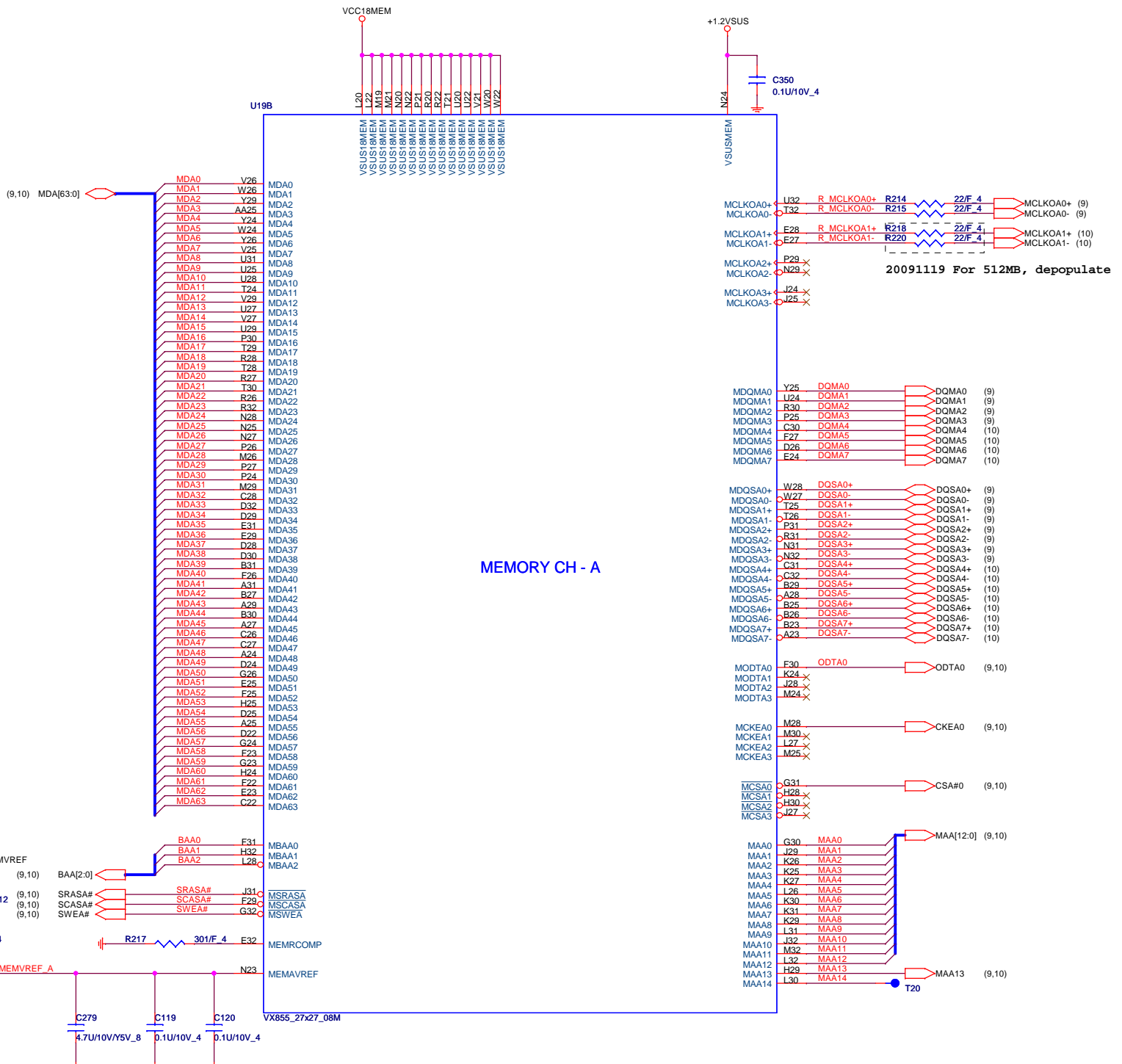


HOST
Rev0.2

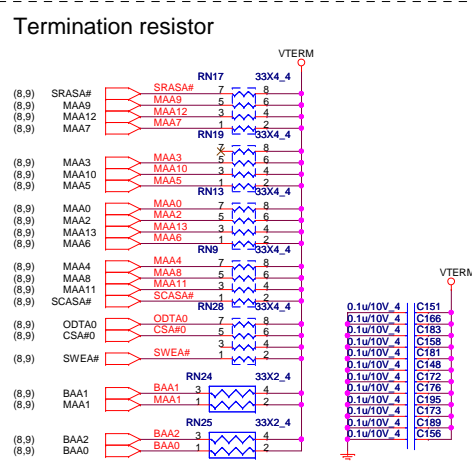
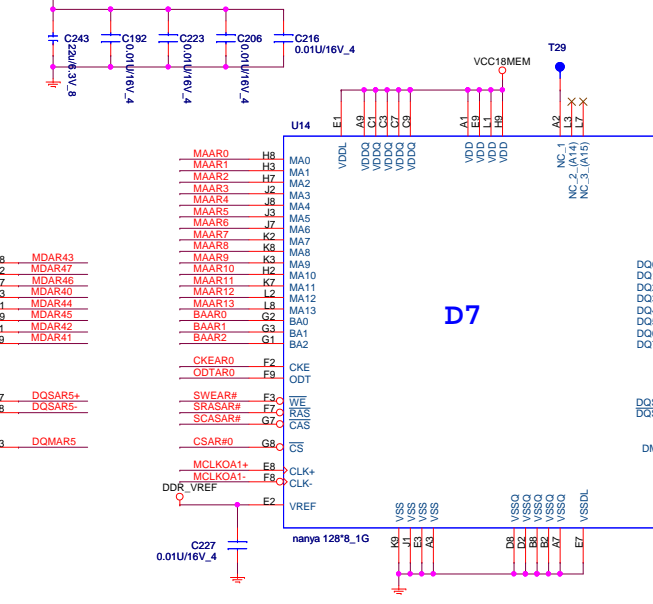
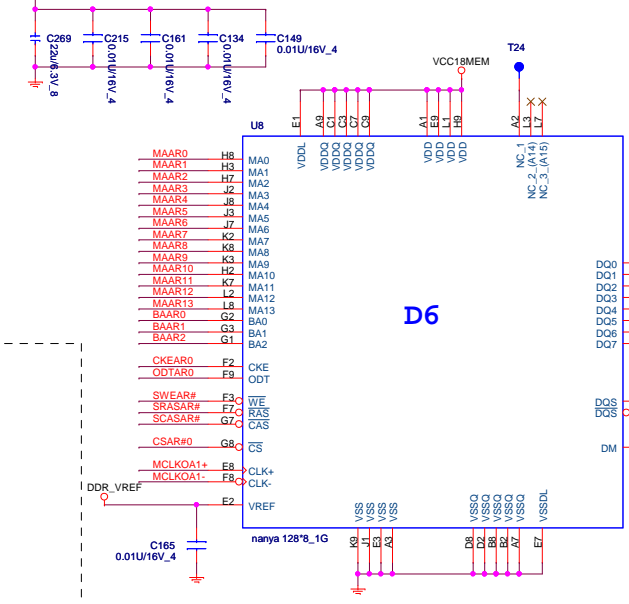
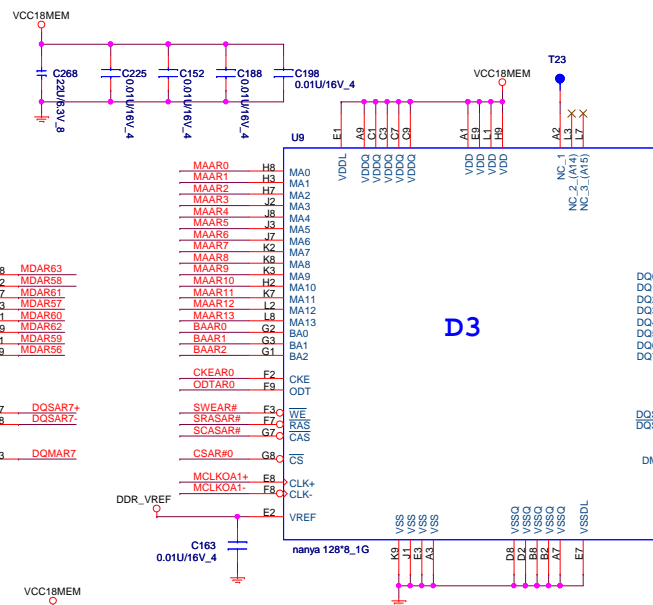
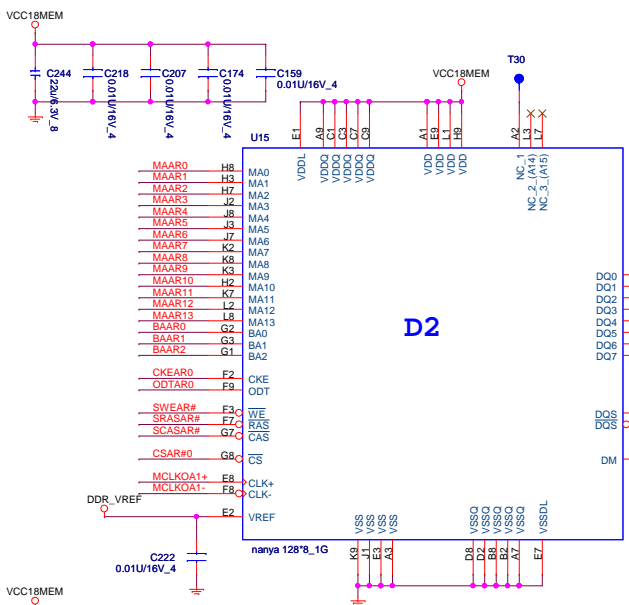
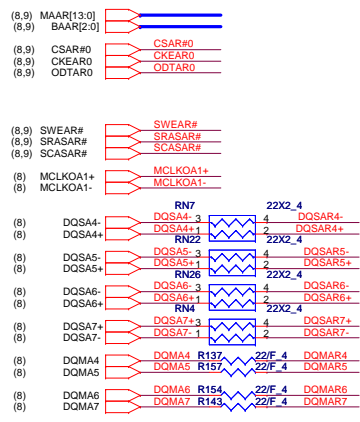


Debug test point



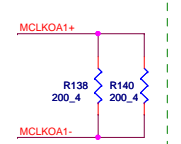


20091119 For 512MB, depopulate

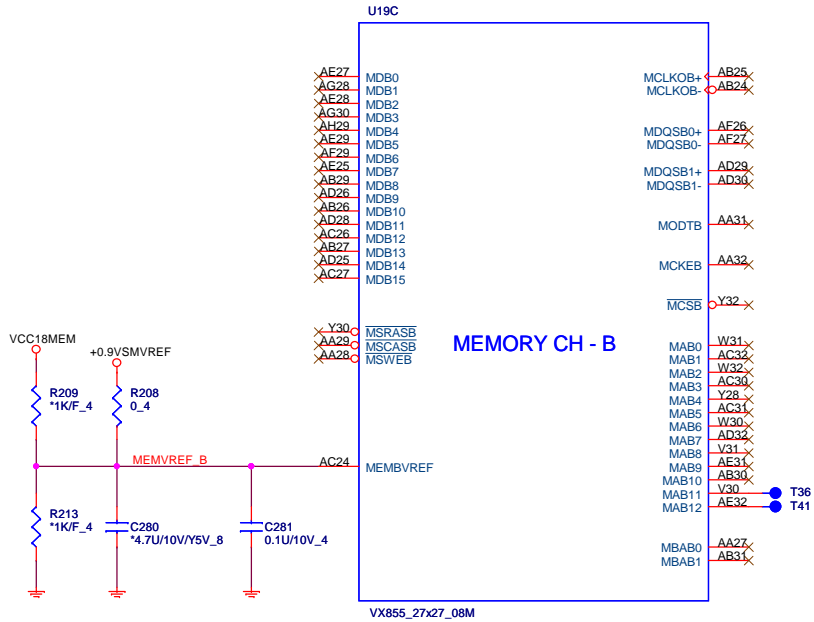


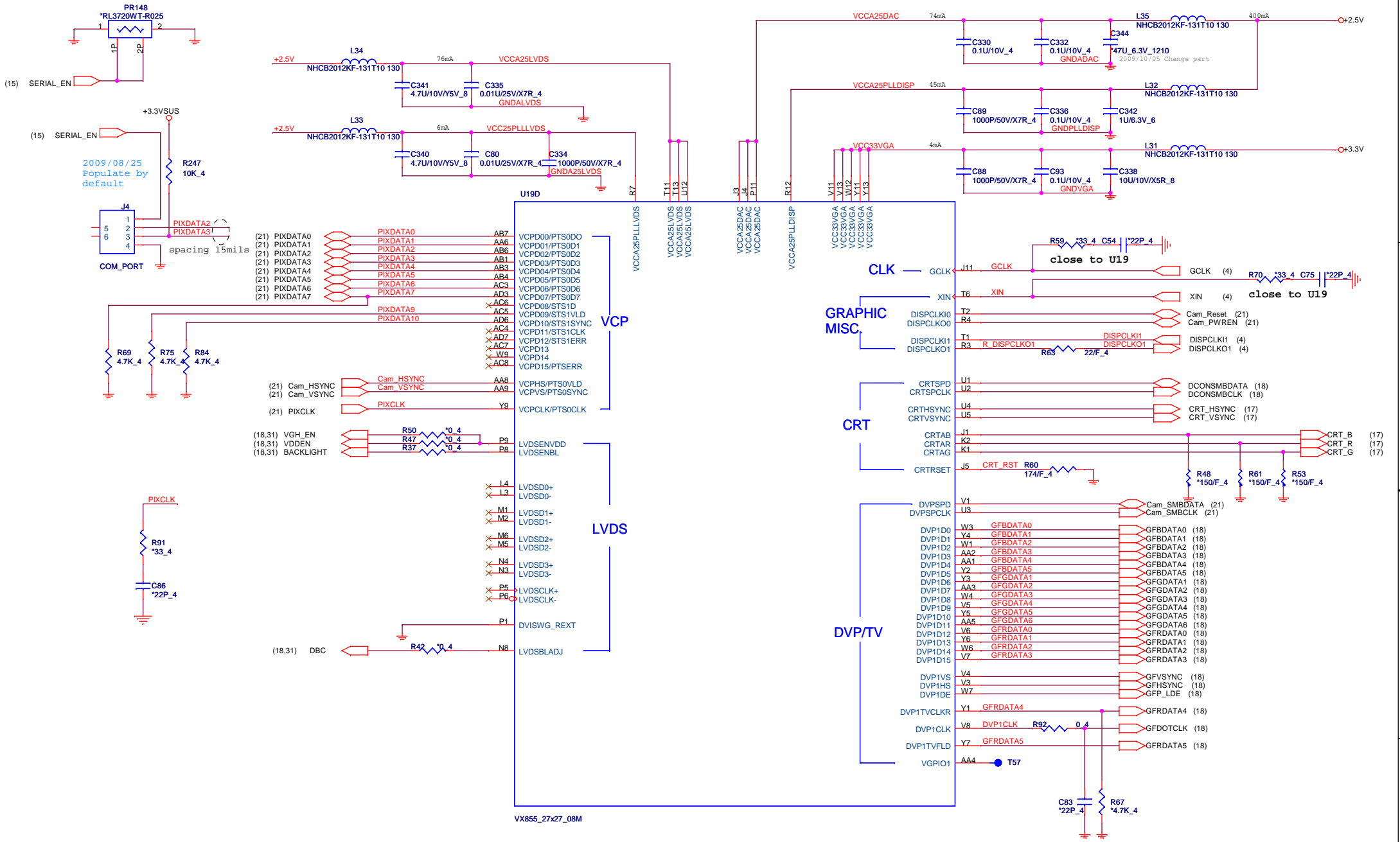
20091119 For 512MB, depopulate

Layout Notes:
 placement between




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 DDR II MEMORY BANK 1



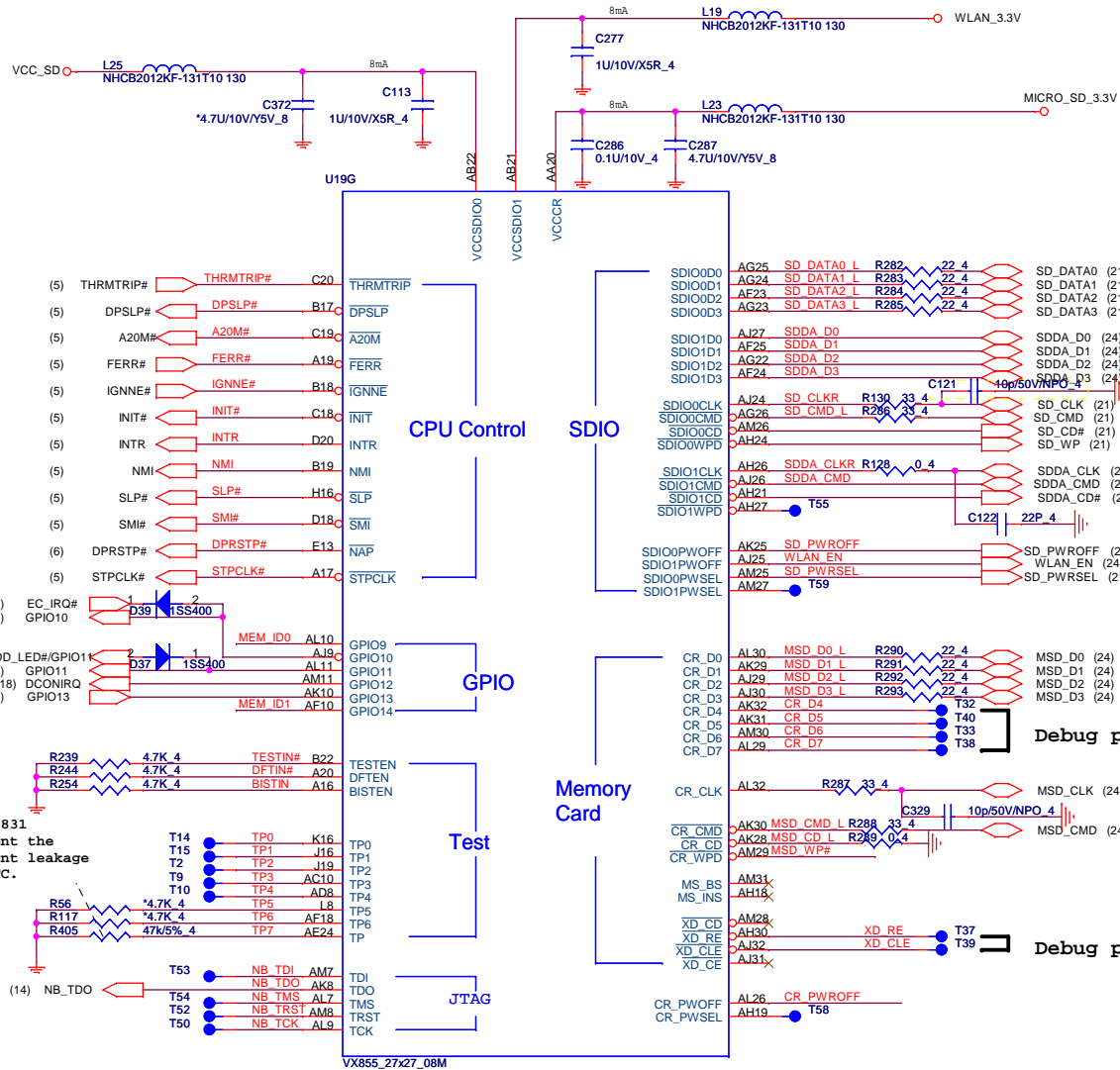


VX855_27x27_08M



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PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) VIDEO BUS	3B
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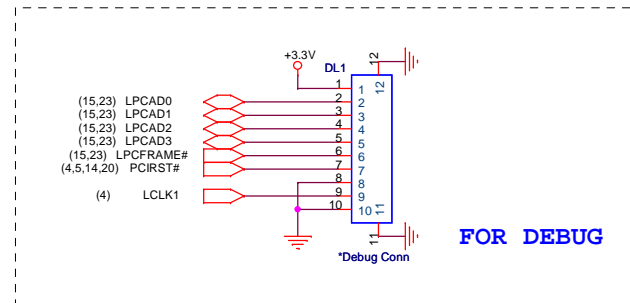
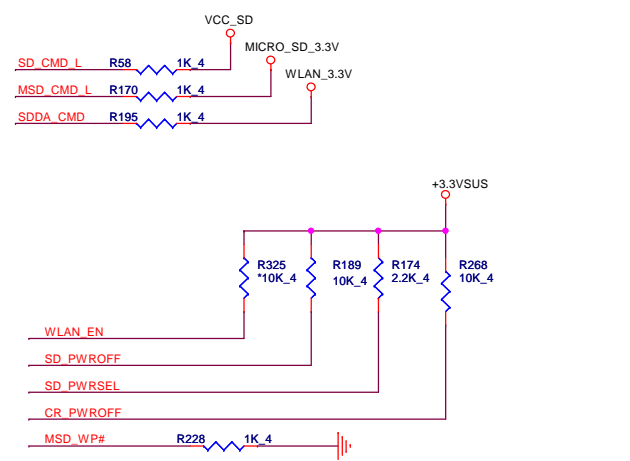
SD Card Reader

WLAN

MICRO SD

Debug port

Debug port



20100831
Prevent the current leakage of RTC.

MEM_ID0	Populate	Depopulate
CL4 (800MHz)	R89	R90
CL3 (667MHz)	R90	R89

MEM_ID1	Populate	Depopulate
1G	R95	R94
512MB	R94	R95

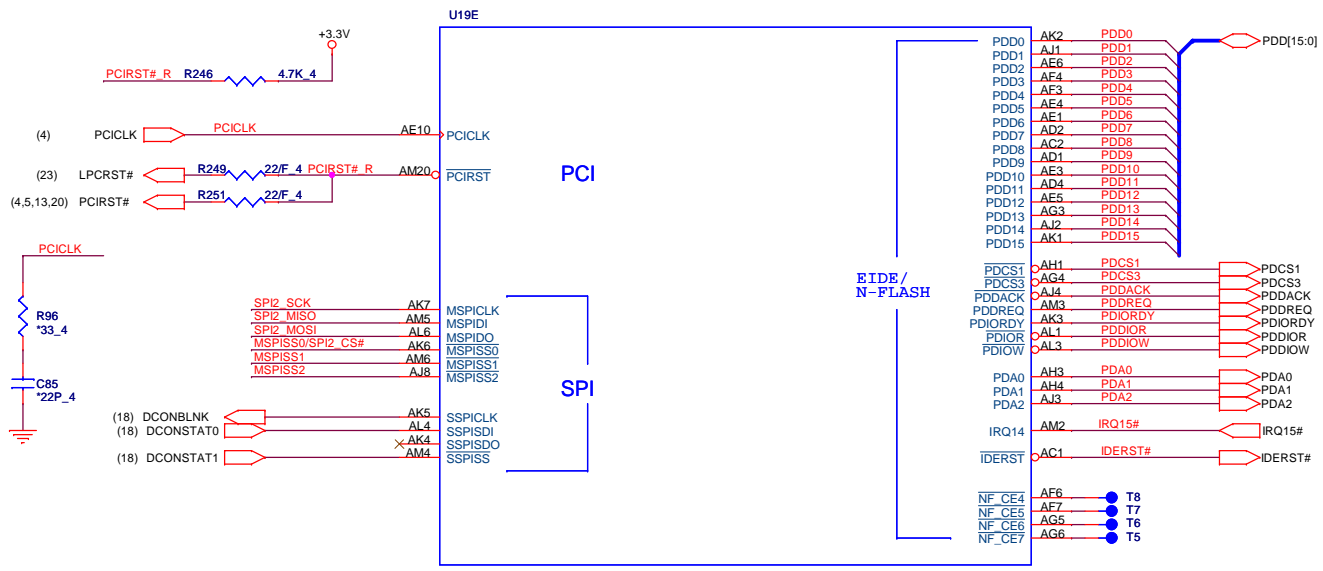
GPIO9/GPIO14 --> Internal pull high(2.5V)

TP2

0 (default)	Normal mode
1	Debug mode

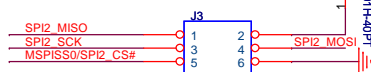
Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) SPI/CARD READER	3B
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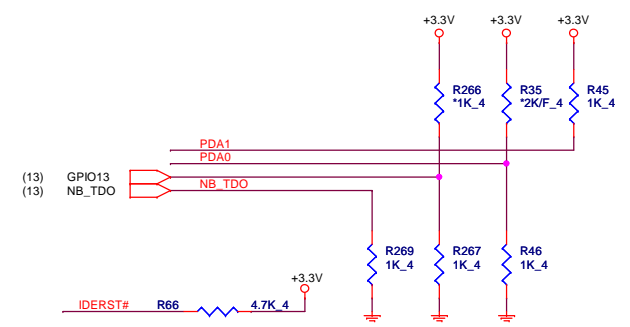
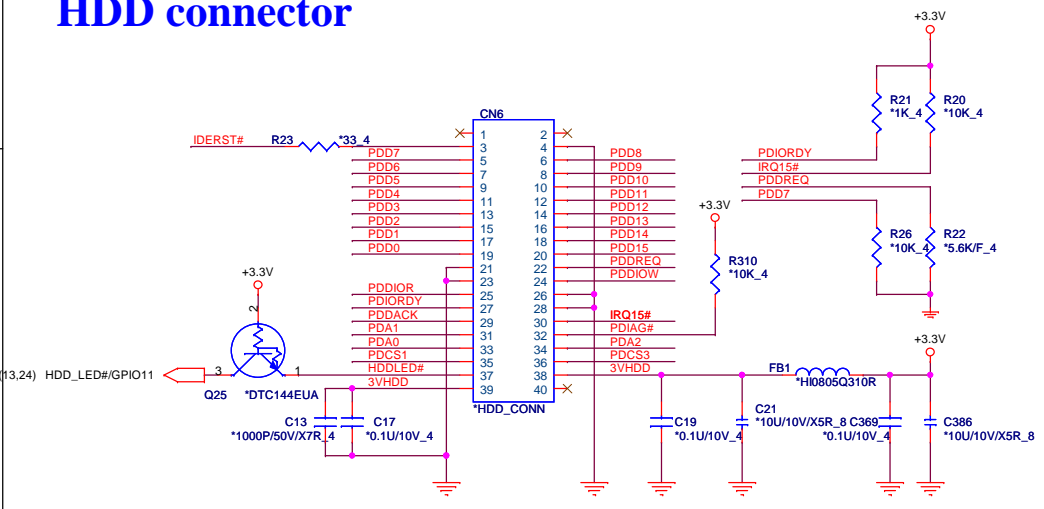
VX855_27x27_08M

Reserve for debug



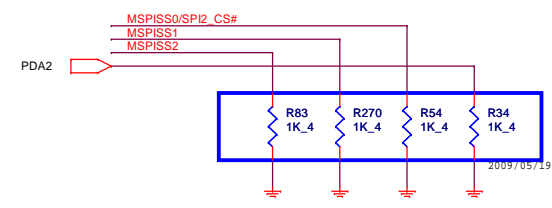
*NA/HEADER 4X2 (Pitch 2.54mm)

HDD connector

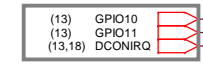


NB Strapping

Pin	Function	Pull Low	Pull High
PDA1	PLL OK source select	from NB PLL	from SB Logic*
PDA0	IOQ depth	12 *	1
GPIO13	GTL pull up	Enable *	Disable
NB_TDO	Debug Link enable	XD Mode*	Debug Link



20091026 modify



2009/05/19 modify

SB Strapping

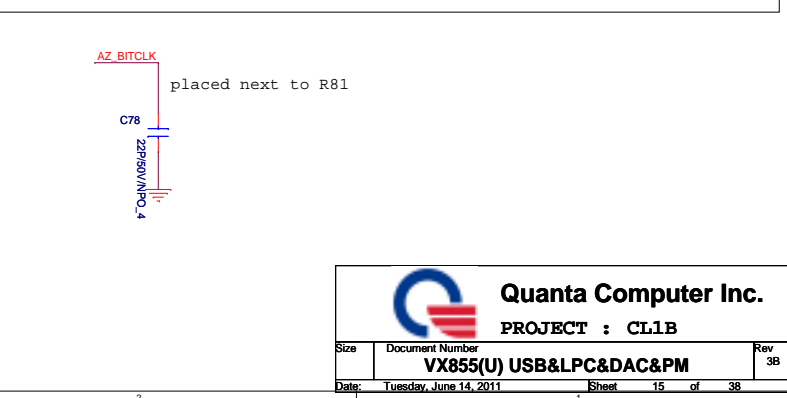
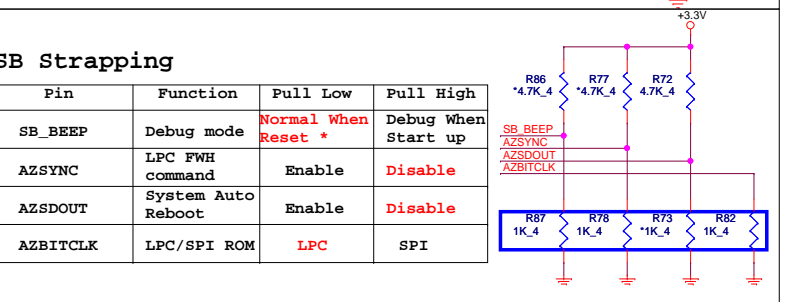
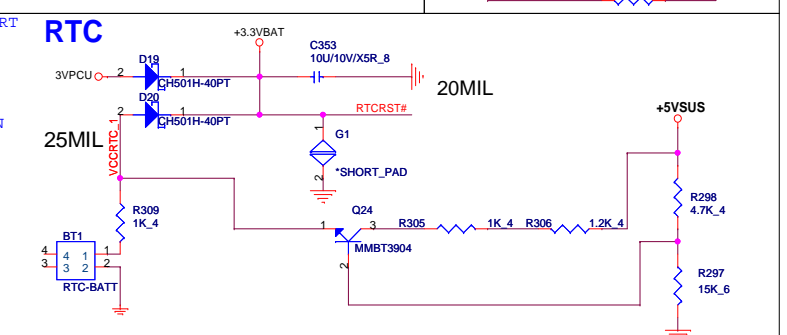
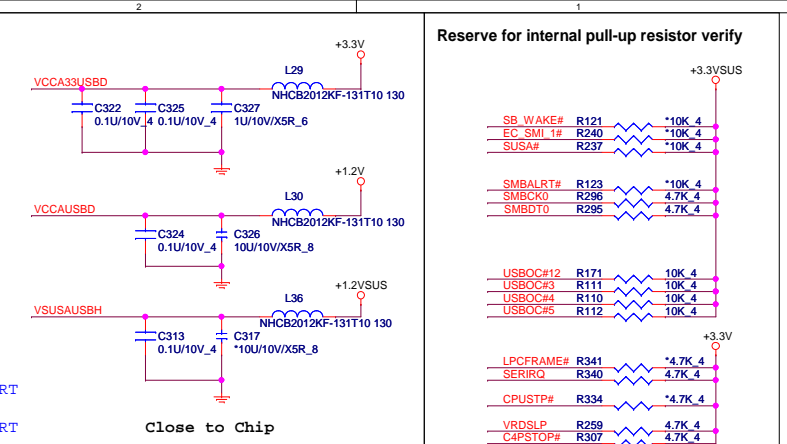
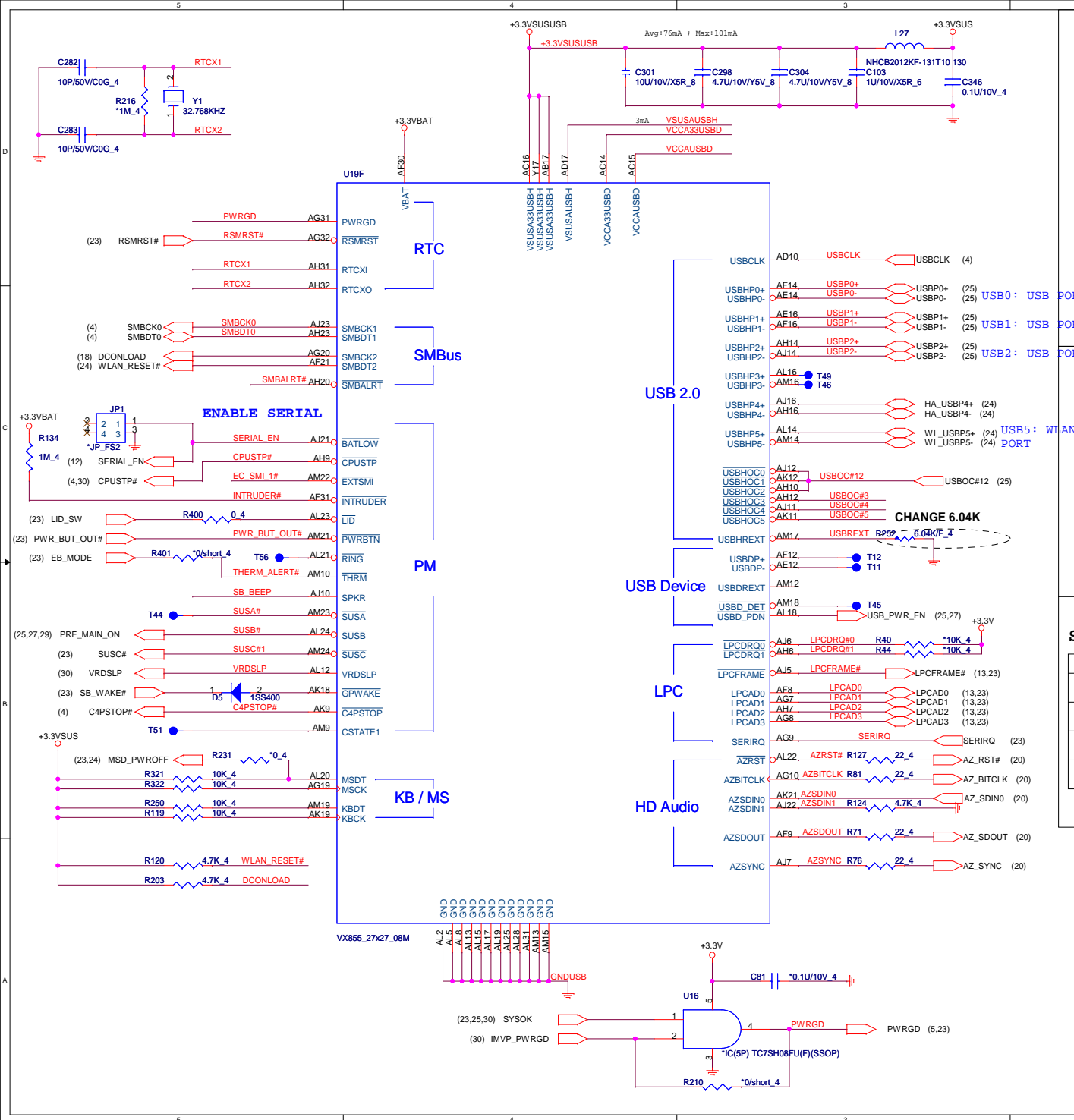
Pin	0:Low 1:High	Function
MSPISS1/ MSPISS0	00 *	IDE
	01	NFC
	10	CE ATA
MSPISS2	0: SPI/LPC *	NFC ROM Select
	1: NFC ROM	
PDA2	0: Disable *	PCI Master Mode Enable
	1: Enable	

NB Strapping

Pin	0:Low 1:High	FSB Freq.
GPIO12/ GPIO11/ GPIO10	000	100Mhz
	001	133Mhz
	010	200Mhz
	011	266Mhz
	111 *	Auto Mode

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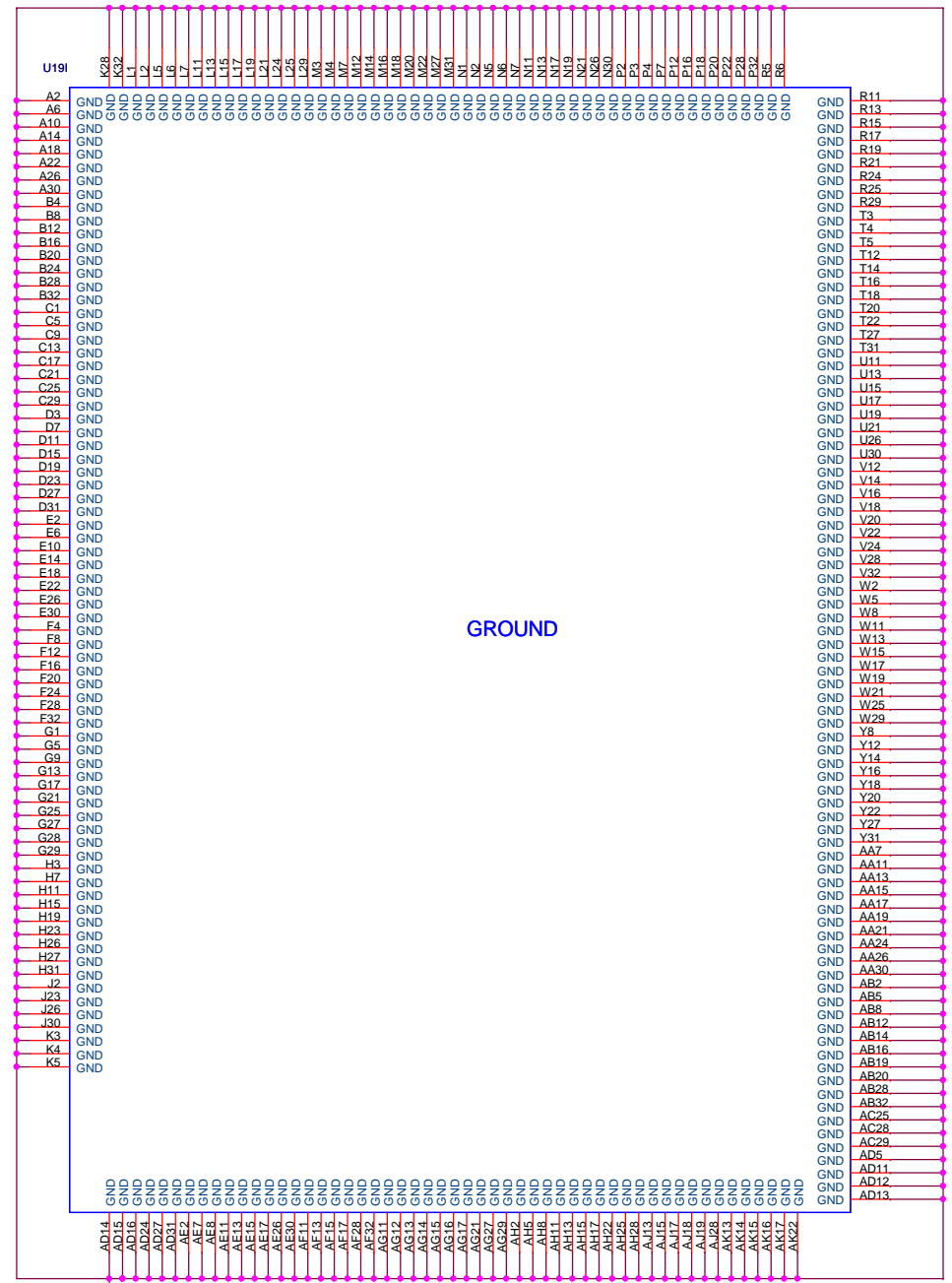
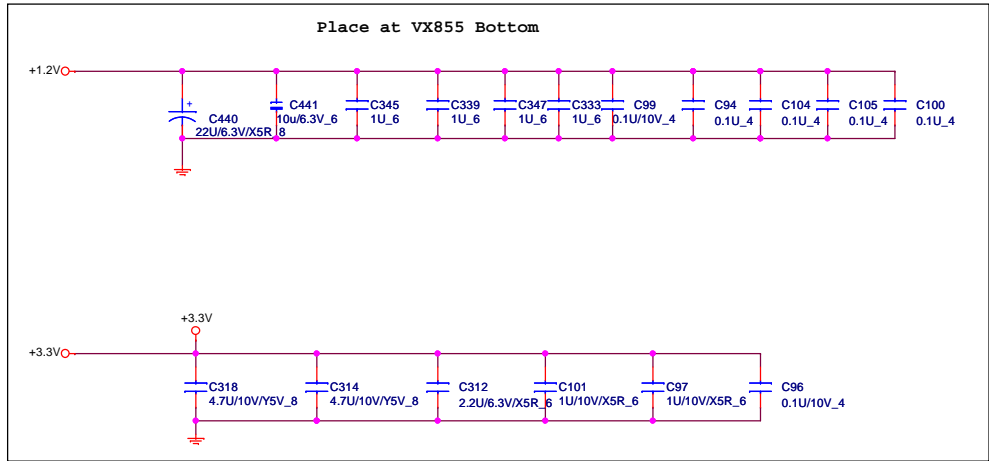
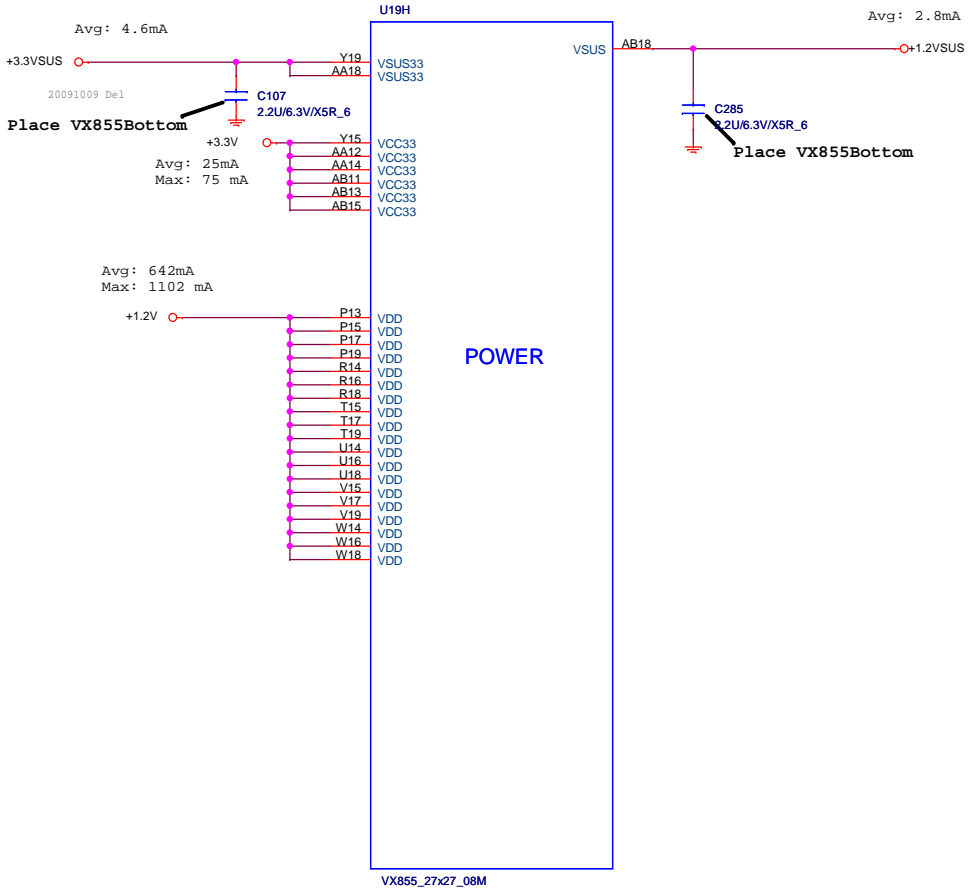
Size	Document Number	Rev
	VX855(U) PCI&PATA&SATA BUS	3B
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Size	Document Number	Rev
	VX855(U) USB&LPC&DAC&PM	3B
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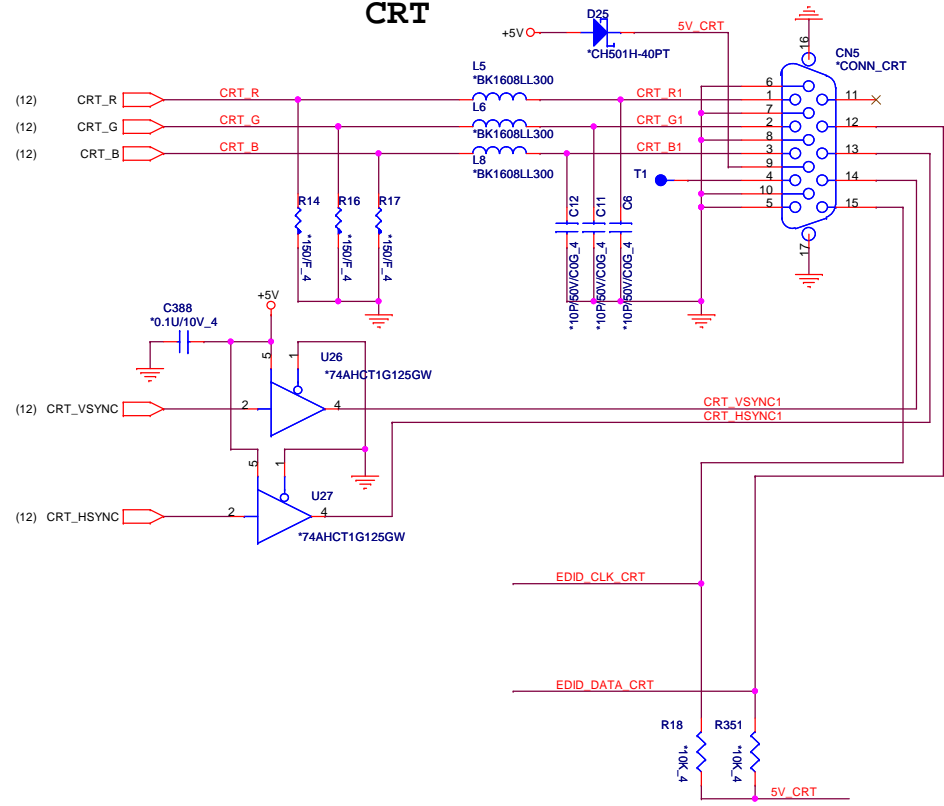
PROJECT : CL1B

Size: Document Number
 Date: Tuesdav, June 14, 2011

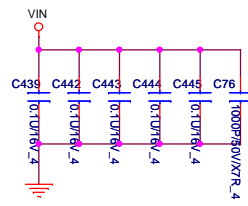
VX855(U) POWER&GND

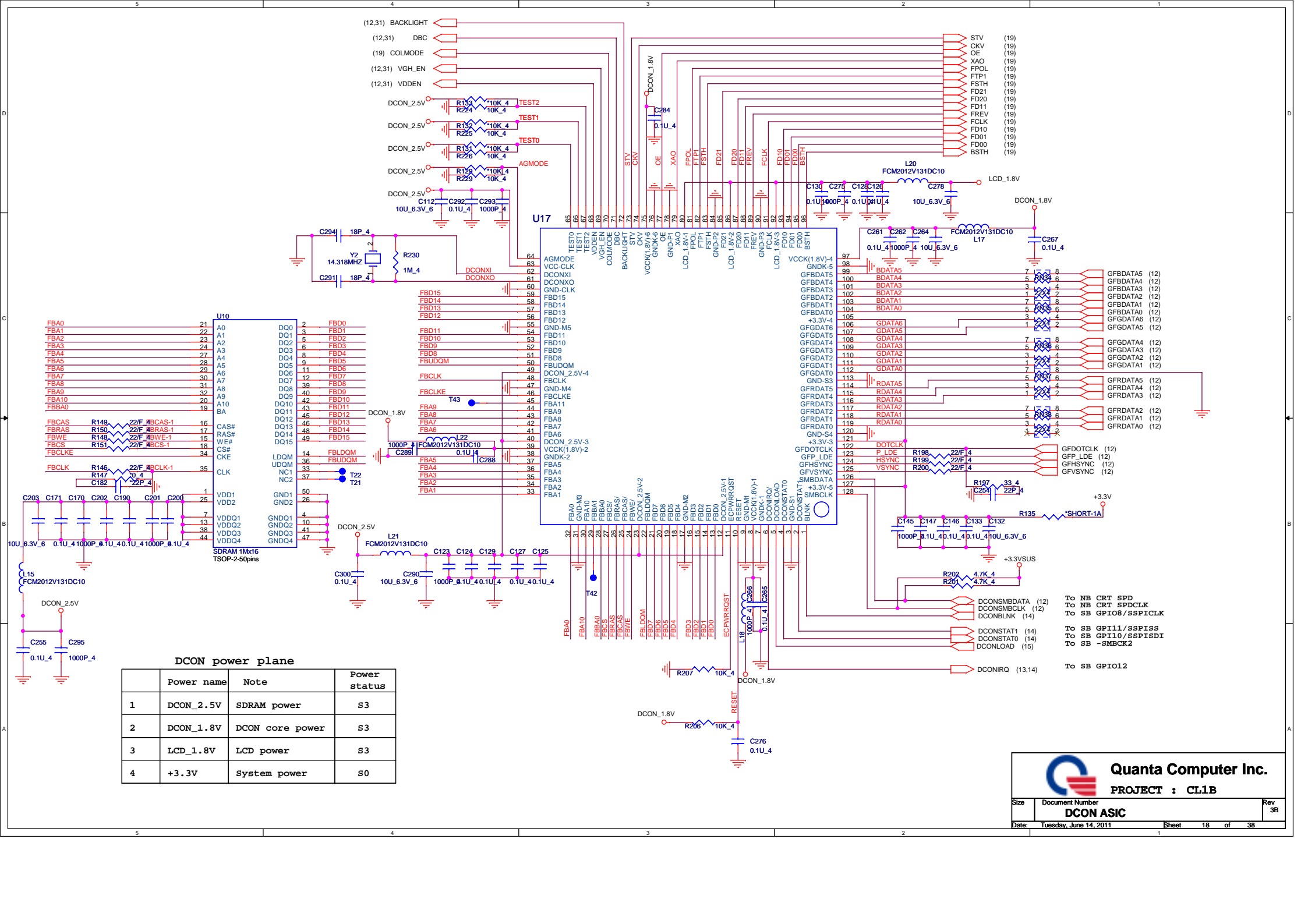
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CRT




EMI





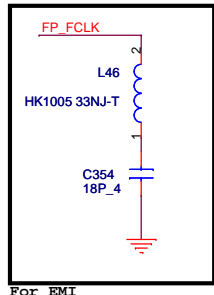
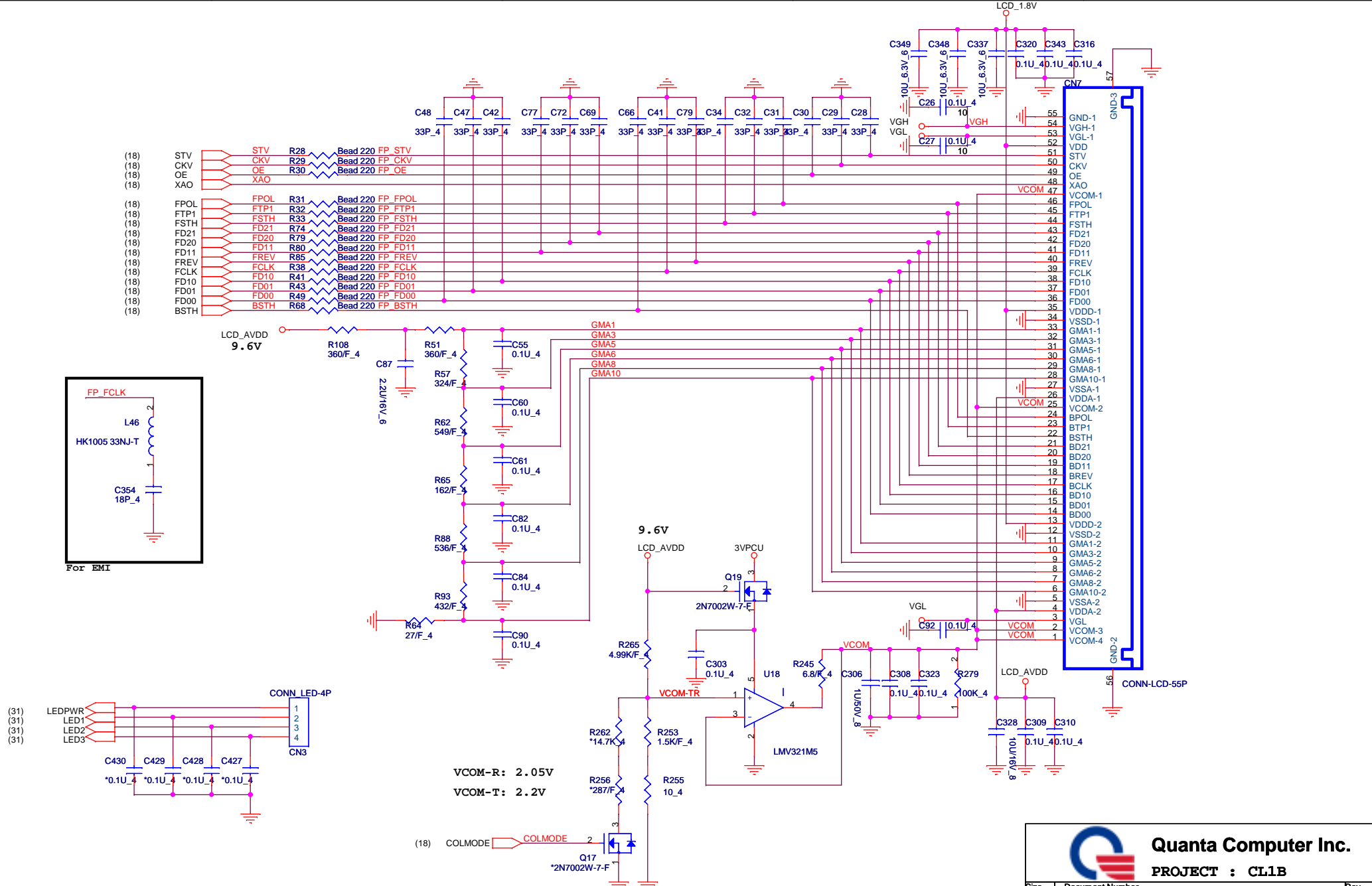
DCON power plane

Power name	Note	Power status
1	DCON_2.5V	SDRAM power S3
2	DCON_1.8V	DCON core power S3
3	LCD_1.8V	LCD power S3
4	+3.3V	System power S0




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Size	Document Number	Rev
DCON ASIC		3B
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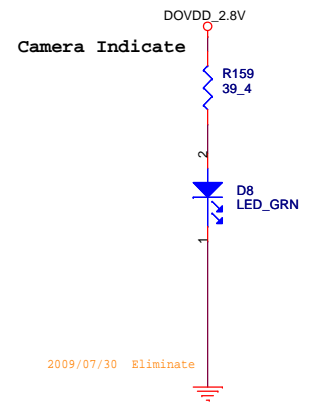
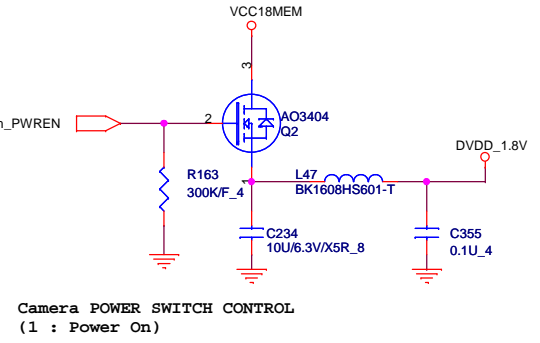
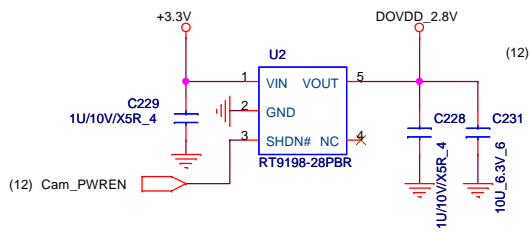
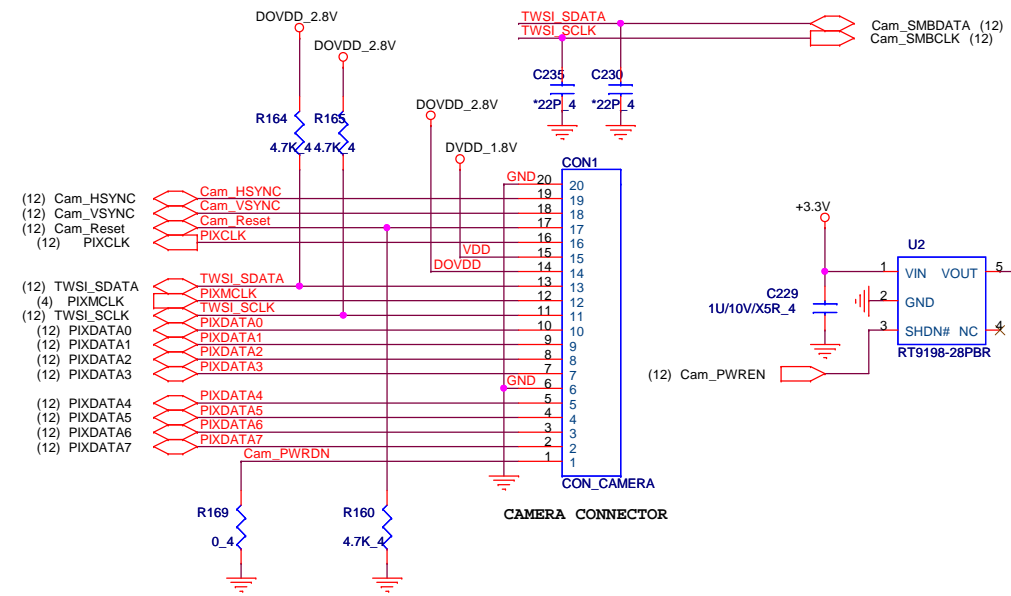
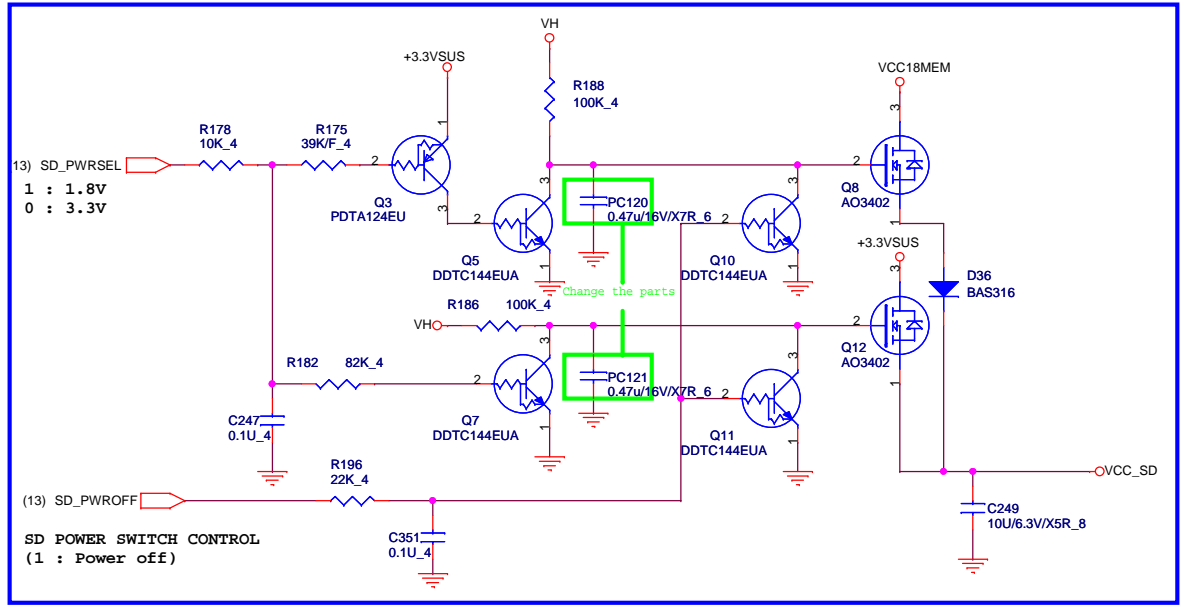
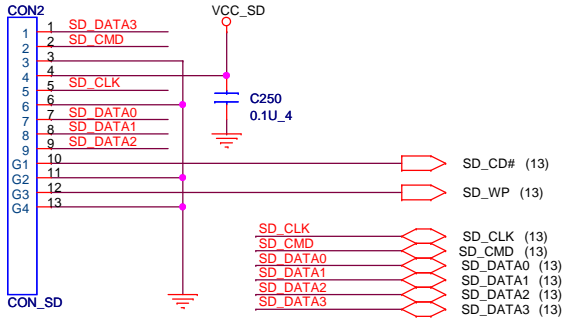


VCOM-R: 2.05V
VCOM-I: 2.2V



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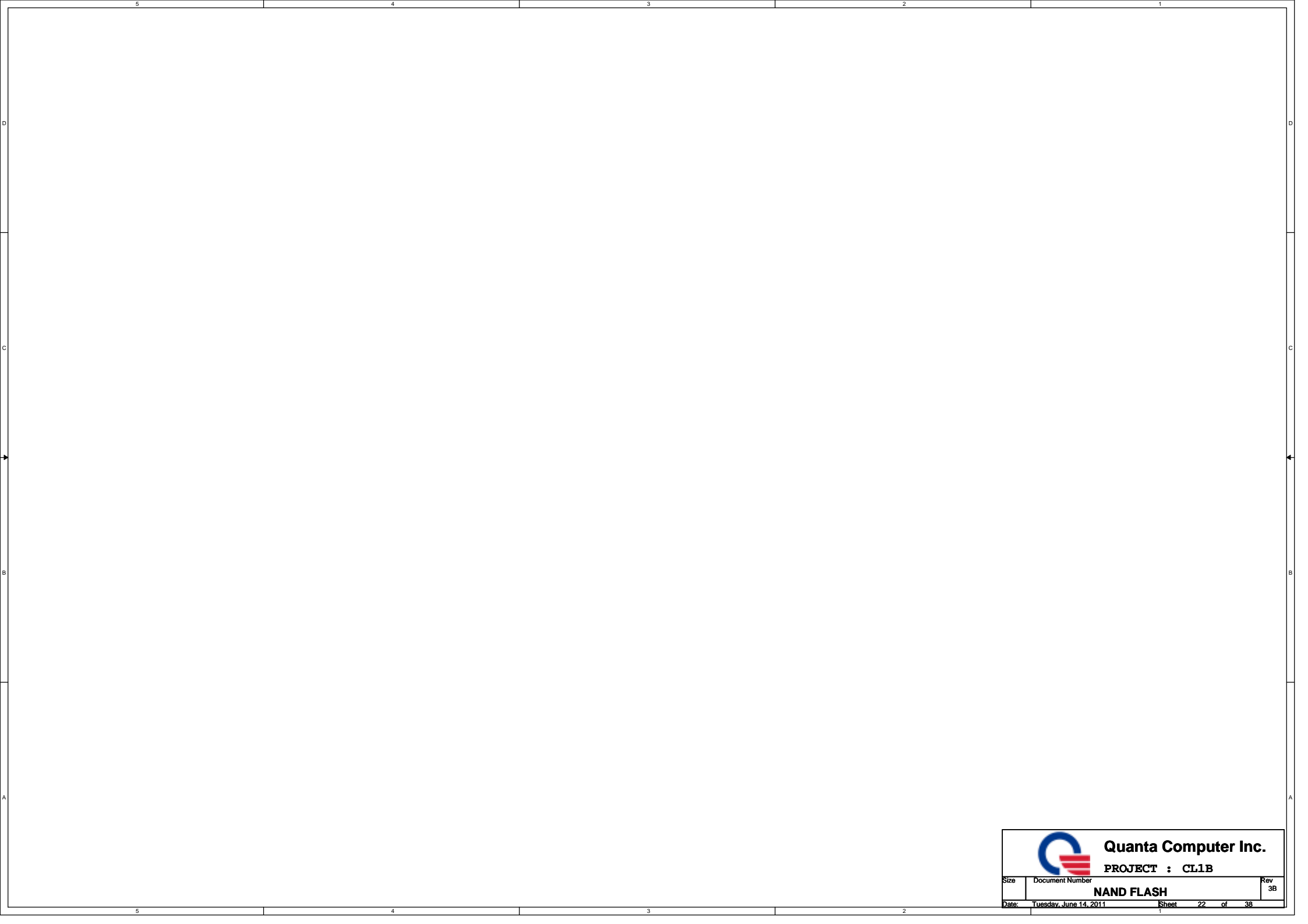
Size	Document Number	Rev
	LCD CONNECTOR	3B
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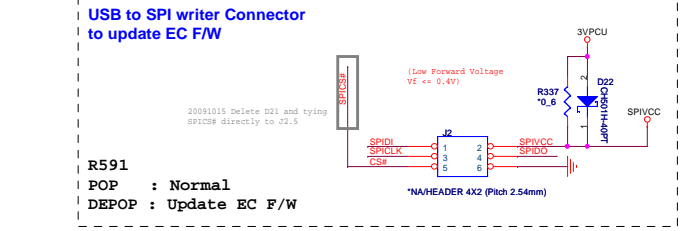
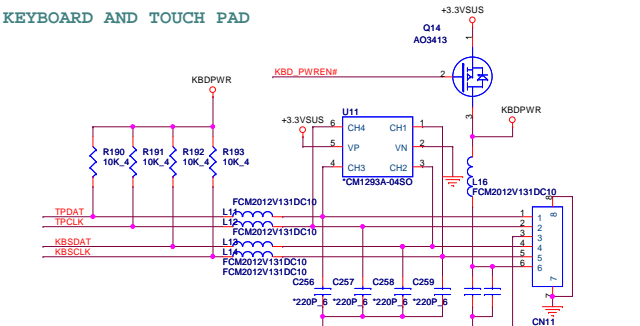
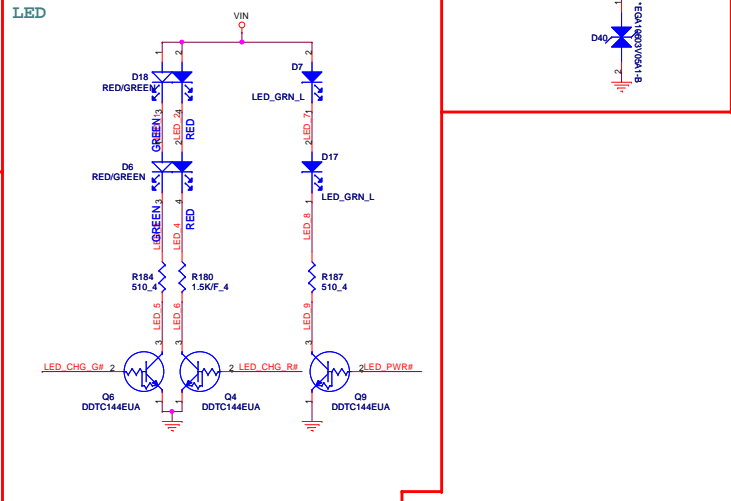
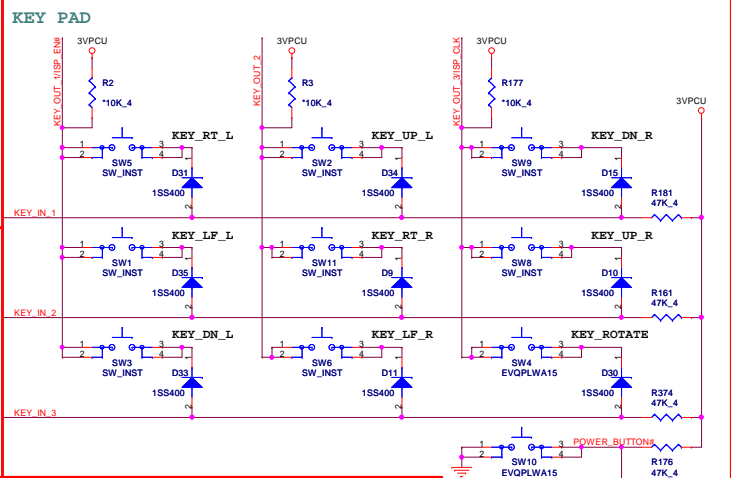
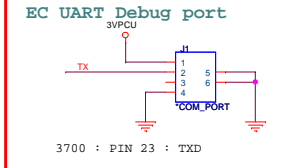
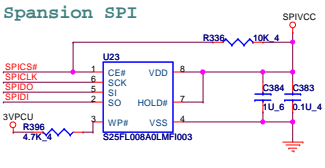
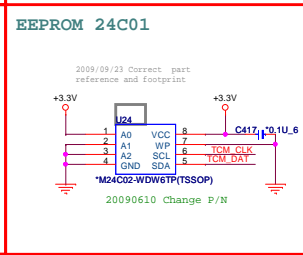
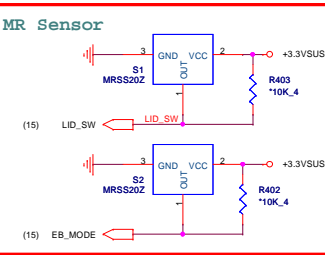
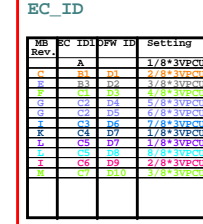
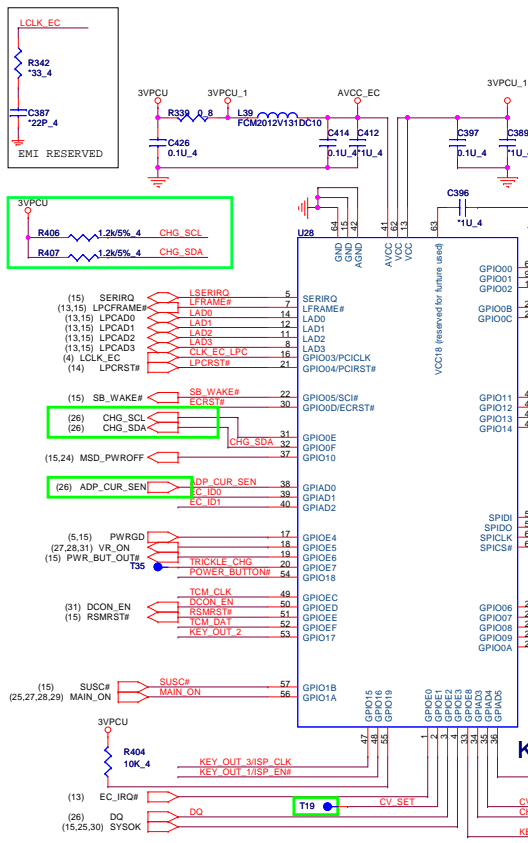
QUANTA CONFIDENTIAL

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NAND FLASH		
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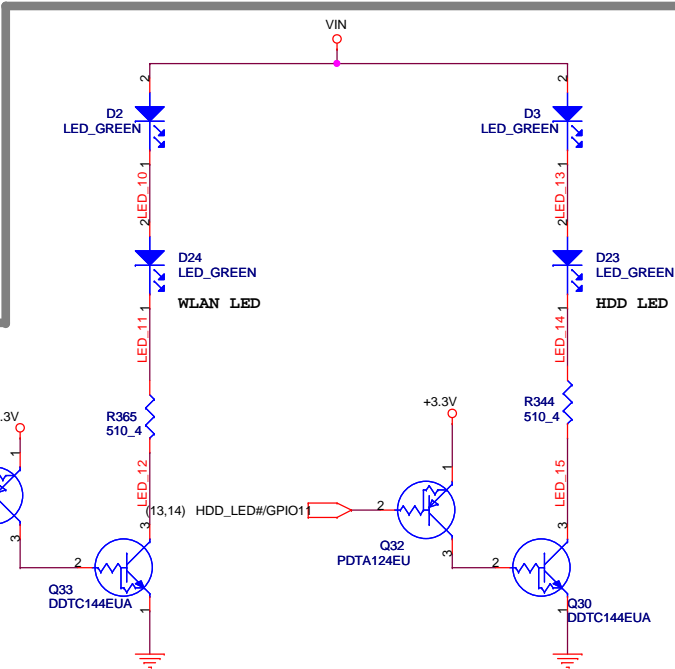
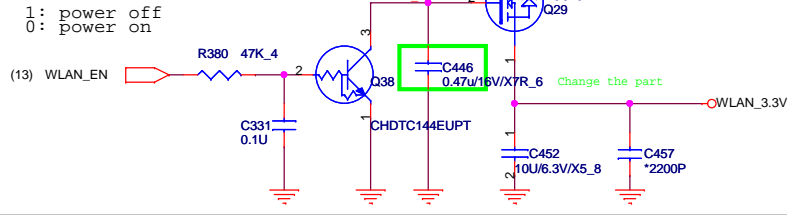
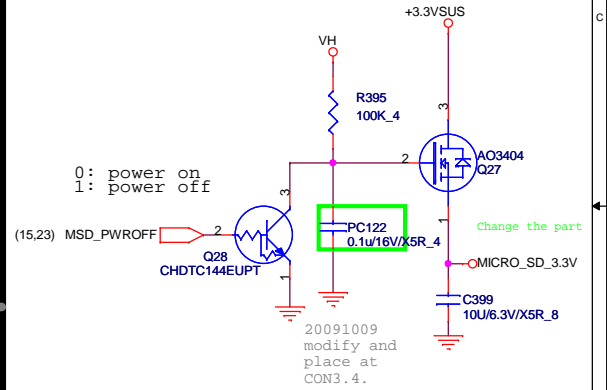
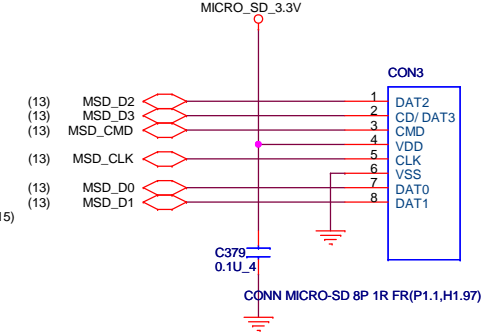
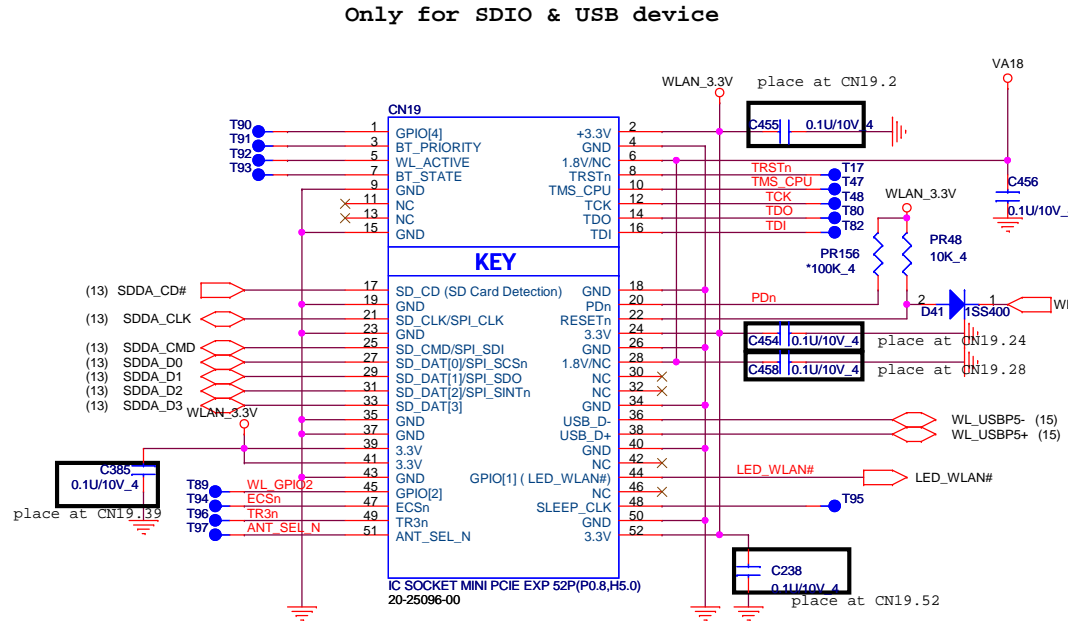


GPIO[2] boot-up configuration:
 0: JTAG mode enabled (pulled low by 100kohms)
 1 and floating: JTAG mode disabled (Default)

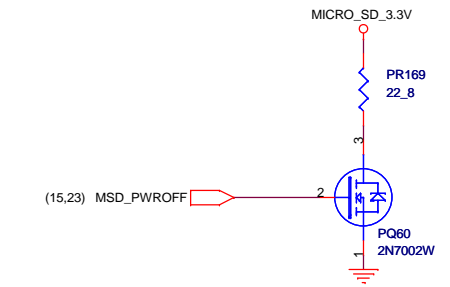
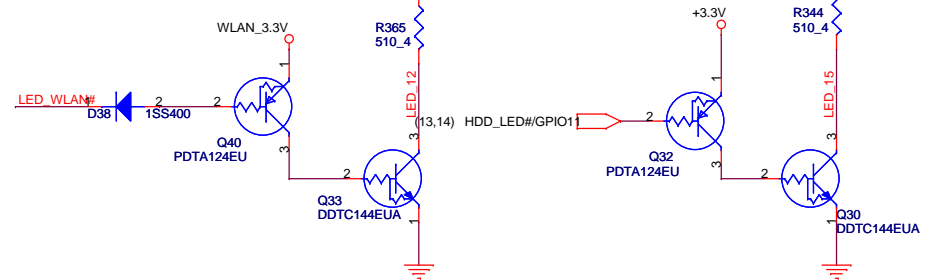
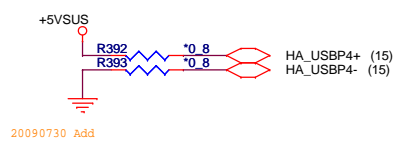
[ANT_SEL_N, TR3n] boot-up configuration:
 00: General SPI (pulled-low by 100kohms)
 11: SDIO (floating is ok)


GPIO[4]:
 WLAN MAC wake-up input/interrupt input

ECSn boot-up configuration:
 0: Boot up from SPI EEPROM (pulled-low by 100kohms)
 1 & floating: Boot up from host interface (Default)



Future Hacking

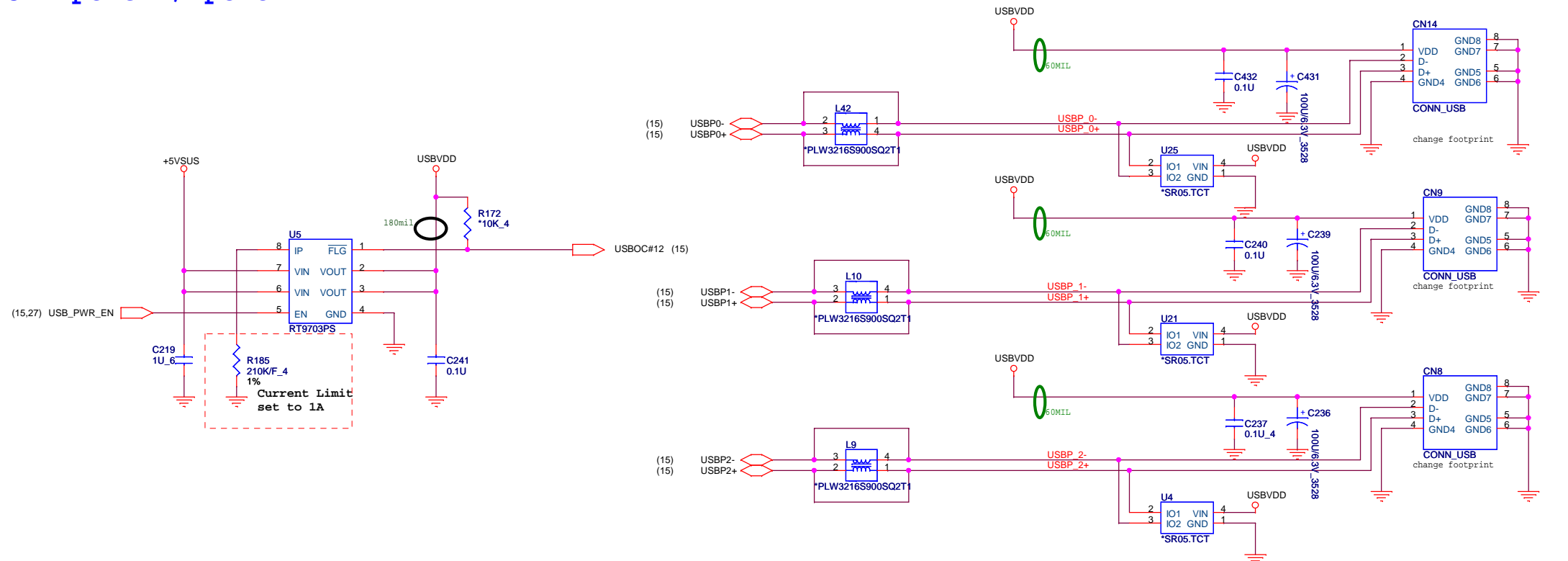




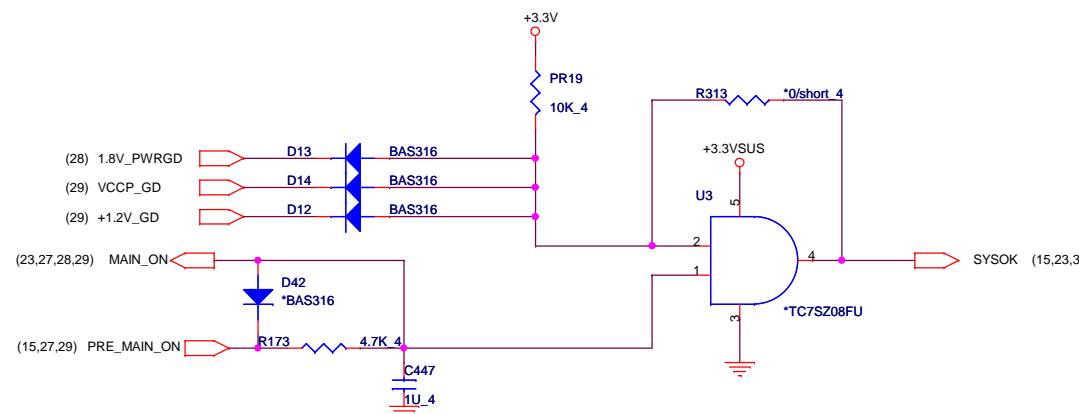
Quanta Computer Inc.
PROJECT : CL1B


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USB power / port



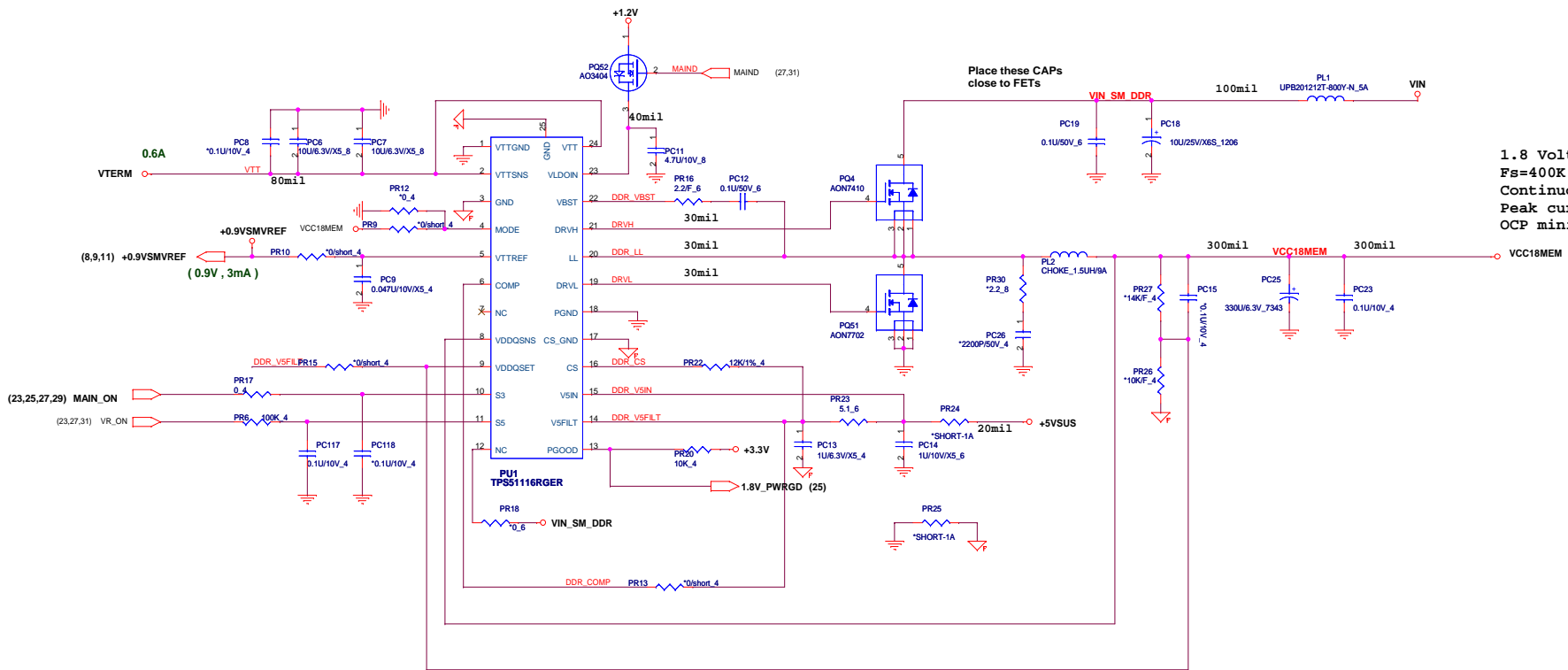
Reset circuit



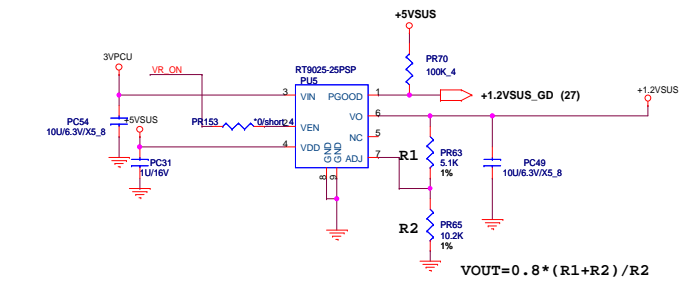
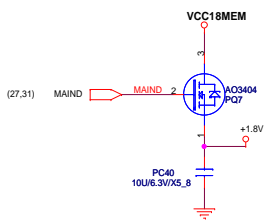


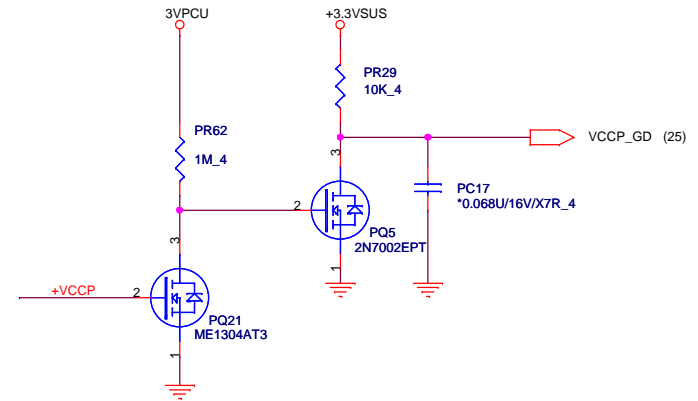
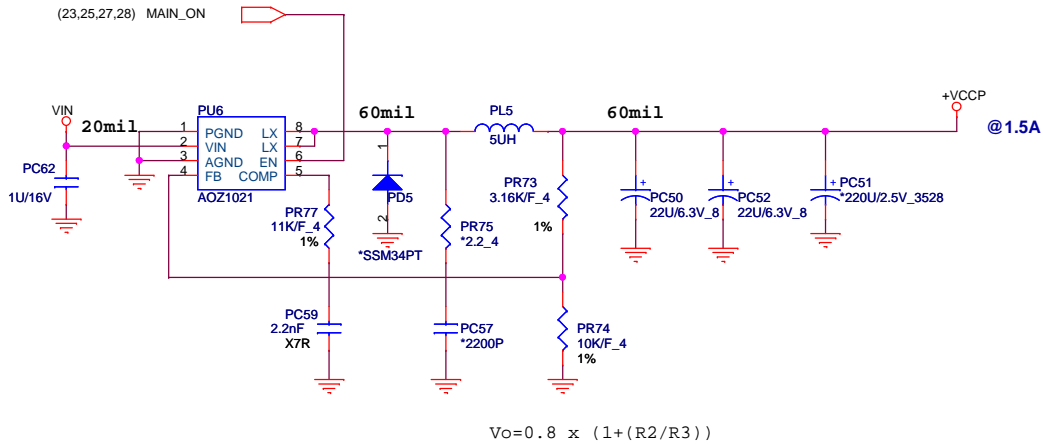
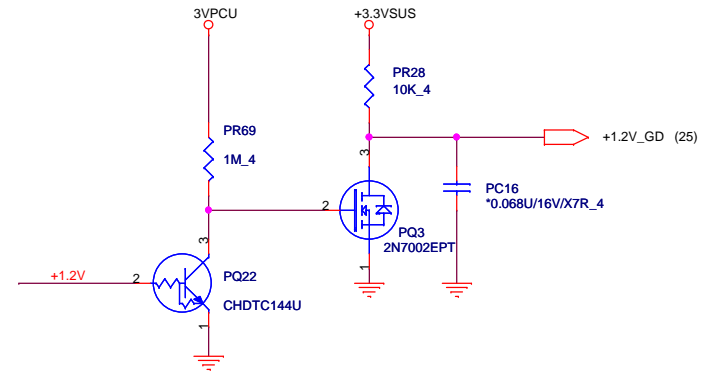
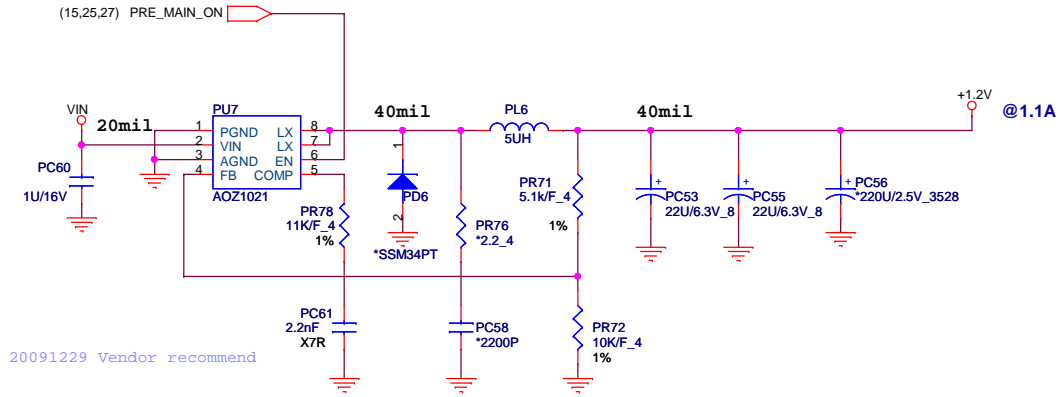
Quanta Computer Inc.
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1.8 Volt +/- 5%
 Fs=400K
 Continuous current:5A
 Peak current:7.5A
 OCP minimum 10A



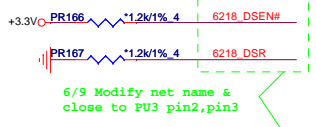


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PROJECT : CL1B

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	DC/DC 1.2V/1.05V	3B
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$I_{ocset} = 1.75V / 175K = 10\mu A$
 $R_{isen} = (I_{oc} * R_{dson} * 0.2175) / (I_{ocset} - 2\mu A - 130)$
 $R_{isen} = (9 * 11m * 0.2175) / (10\mu A - 2\mu A) - 130 = 2.56K$

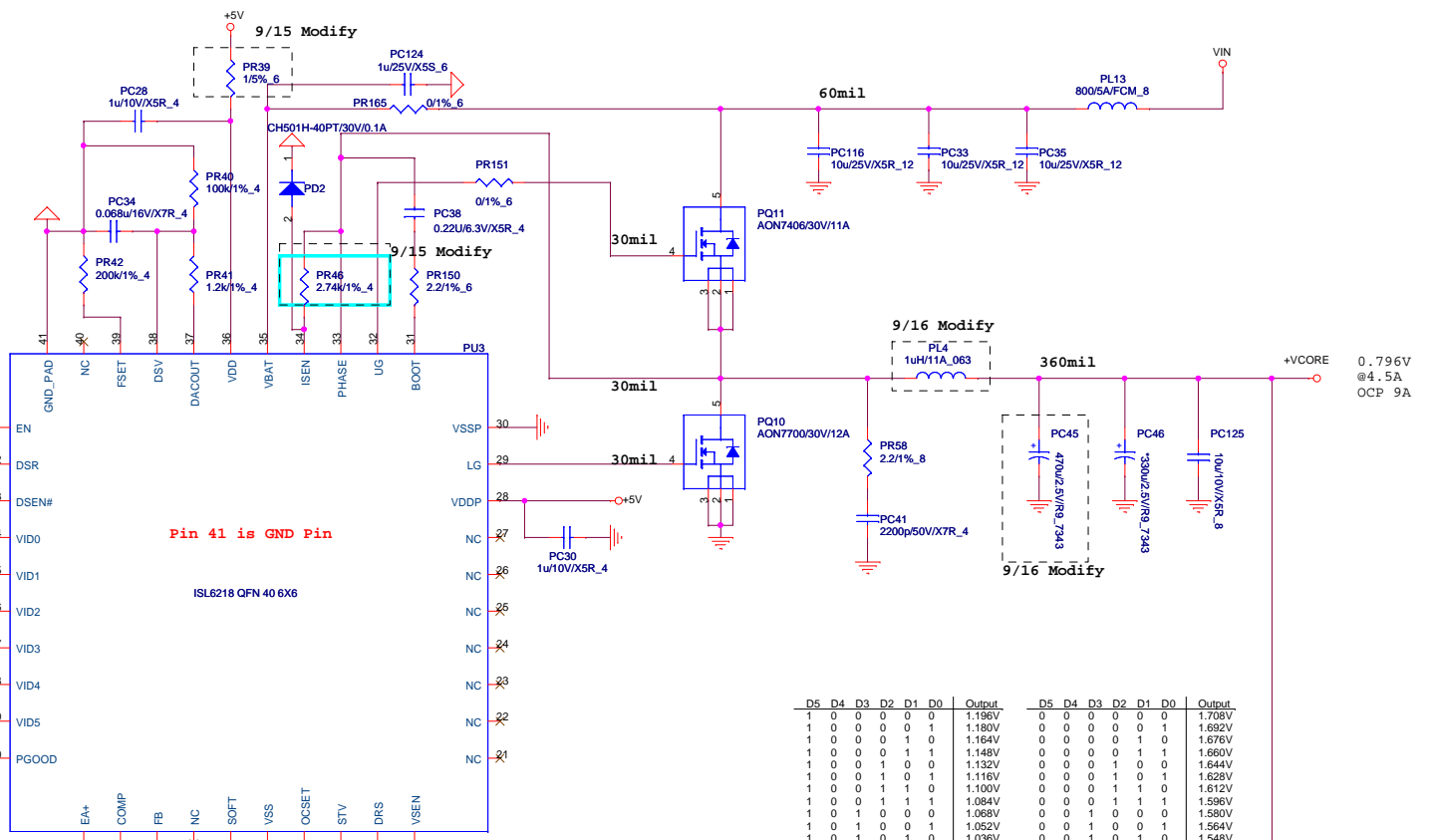


6/9 Modify net name & close to PU3 pin2, pin3

VID0-VID5 do not have internal pull-up or pull-down capability.

$R_{pullup} = V / (2.6mA - r_{dson}) = (3.3 - 0.05 * 3.3) / (3m - 15) = 1.33K$

$R_{droop} = 2.3 * Droop * R_{isen} / R_{dson}$
 $R_{droop} = 2.3 * 0.001 * 3.32K / 14m = 545ohm$



Pin 41 is GND Pin


ISL6218 QFN 40 6X6

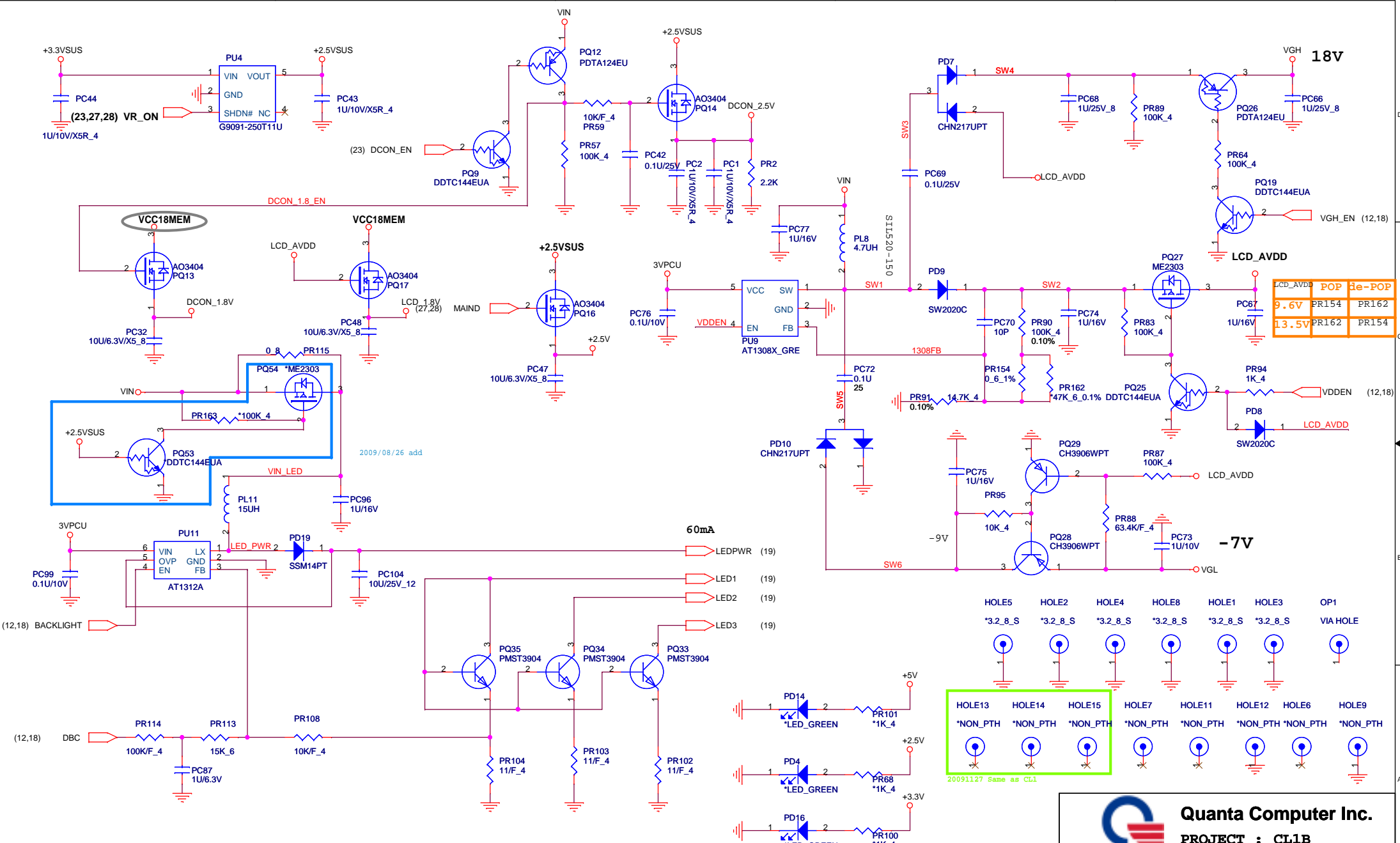
VCC BOOT : 1.201V

CPUSTP#	VRDSLPL	MODE OF OPERATION	OUTPUT VOLTAGE
1	0	Active	VID
X	1	Deep sleep	0.732V

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	1	1	1	1.148V	0	0	0	1	1	1	1.660V
1	0	1	0	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	1	0	1	1	1.116V	0	0	0	1	1	1	1.628V
1	0	1	1	0	0	1.100V	0	0	0	1	1	0	1.612V
1	0	1	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	1	1	1.052V	0	0	1	0	1	0	1.564V
1	0	1	1	0	1	1.036V	0	0	1	1	0	1	1.548V
1	0	1	1	1	1	1.020V	0	0	1	1	1	1	1.532V
1	0	1	0	0	0	1.004V	0	1	0	0	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	1	1	0.924V	0	1	0	0	1	1	1.436V
1	1	0	1	0	0	0.908V	0	1	0	1	0	0	1.420V
1	1	0	1	1	1	0.892V	0	1	0	1	1	1	1.404V
1	1	1	0	0	0	0.876V	0	1	1	0	0	0	1.388V
1	1	1	0	1	1	0.860V	0	1	1	1	0	1	1.372V
1	1	1	1	0	0	0.844V	0	1	1	1	0	0	1.356V
1	1	1	1	1	1	0.828V	0	1	1	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	1	1	0.796V	0	1	1	0	1	1	1.308V
1	1	1	1	0	1	0.780V	0	1	1	1	0	1	1.292V
1	1	1	1	1	0	0.764V	0	1	1	1	0	1	1.276V
1	1	1	1	1	1	0.748V	0	1	1	1	1	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

6/9 PR152 change from short pad to not stuff & add PR135, PR136 for C3/C4 hang up issue


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 PROJECT : CL1B
 DC/DC CPU CORE (ISL6218)
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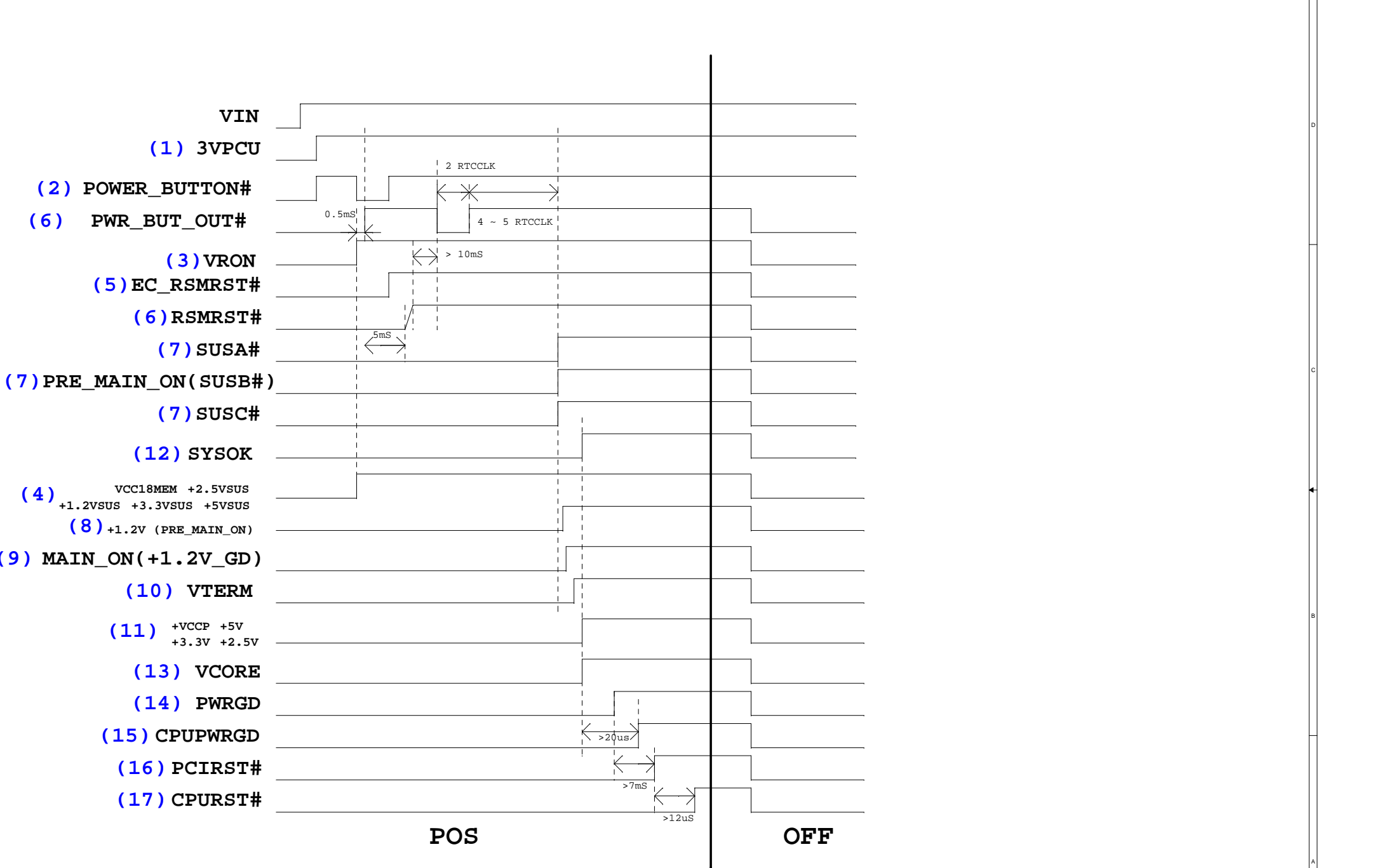


HOLE5	HOLE2	HOLE4	HOLE8	HOLE1	HOLE3	OP1
*3.2_8_S	*3.2_8_S	*3.2_8_S	*3.2_8_S	*3.2_8_S	*3.2_8_S	VIA HOLE
HOLE13	HOLE14	HOLE15	HOLE7	HOLE11	HOLE12	HOLE6
*NON_PTH	*NON_PTH	*NON_PTH	*NON_PTH	*NON_PTH	*NON_PTH	*NON_PTH

20091127 Same as CL1

Quanta Computer Inc.
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	VEE / BL	3B
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Schematic modify Item and History :

A1-->A2

1. DCON POWER -

- A. Change PQ9.B pin from DCON_1.8 to DCON_EN
- B. Change PQ13.G pin from DCON_EN to PQ12.C
- C. Change PQ17.G pin from VDDEN to LCD_AVDD

2. SB straping -

- A. Change R27, R83, R270, R54, R34, R87, R78 and R82 from 4.7K ohm to 1K ohm.

3. Design issue -

- A.The D pin and S pin of Q8 and Q12 is inverse
- B.Change C299 part number
- C.Add test points: U28, pins 1, 4, 17, 29, 36, and 37
- d.Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L
- e.RTC issue: VIA recommend to delete R216

4. Power -

A.1.8VSUS

- a. Add off-page connector : VR_ON
- b. Modify PU5 pinout.
- c. For +1.8VUSU sense: stuff PR15 ; don't stuff PR27 and PR26
- d. For +1.8VUSU OCP : modify PR22 from 4.99K to 6.2K, OCP from 3A to 3.5A
- e. modify PU1 pin11 net name to VR_ON

B.+VCORE:

- a.For SYSOK PULL HIGH: Stuff PR45
- b.For +VCORE sense: don't stuff PC3 & PR3 ; stuff PR51 & PR52
- c.For CPU Load line : for meet load line -1mV/A, modify PR52 & PR50 from 1K to 680 ohm

C.1.2 and +VCCP:

- a.Modify power good circuit: change net name from 3.3VSUS to +3.3VSUS

D.Charger :

- a.Delete clamp circuit (PR118,PD18,PQ38,PR124):
PUL2 (MB39A129) can guaranty to 28V
- b.connect PUL2 pin21 to PQ36 pin1,2,3 directly
- c.change PR126 to 100K

5.WLAN-

- Change WLAN solution from SD card to TM100 module. See page 24



Quanta Computer Inc.

PROJECT : CL1B

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Schematic modify Item and History :

A2-->B1

2. SDIO

- A. SDIO:Micro SD
- B. SDIO1: SD Card Reader
- C. SDIO2: WLAN module

2. SB straping -

- A. Change R58, R170 and R195 pull up power plane on page13

3. Design issue -

A.Modify CPU RST circuit

- a.Add R248 0 ohm
- b.Populate Q18,Q20 R275 to prevent leakage for vendor's recommand.
- c.Del c299 for CPU power good delay time

B.Del SPI ROM of memory

C.Modify DCONLOAD and WLAN_RESET# to U19.AG20 and AF21

D.Modify Serial enable to U19.AJ21

E.Modify THRM# pin of U19 from PROCHOT# to EB_MODE

F.Del EDID_CLK and EDID_DATA of CRT circuit

G.Del R195 within GDATA0 pull low

H.Rerevse C436,C438, C233 and C232 for EMI/ESD

I.Add PC120 and PC121 for VH gilch and add D36 to prevent 3VPU forward to +1.8VSUS

J.Move C250 to close CON2 and modify CAM LED control.

K.Del NAND flash on page 22

L.Add PWRGD net on U28.17 & SYSOK on U28.4 & change M/B ID & Del SW7 on page 23

M. change Q14 from PNP BJT to P-MOS

N. Change WLAN solution from on board to slot and correct WLAN LED behavior on page 24.

O. Add Micro SD on page 24.

P. Correct power good circuit on page 25.

4. Power -

A.Del all jump,but only reserve the jump of +VCCORE and +1.8VSUS.


A.1.8VSUS

- a. Add off-page connector : VR_ON
- b. Modify PU5 pinout.
- d. For +1.8VUSU OCP : modify PR22 from 4.99K to 6.2K, OCP from 3A to 3.5A

B.+VCCORE:

- a.For SYSOK PULL HIGH: Stuff PR45
- b.For +VCCORE sense: don't stuff PC3 & PR3 ; stuff PR51 & PR52
- c.For CPU Load line : for meet load line -1mV/A, modify PR52 & PR50 from 1K to 680 ohm

D.Charger :

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		3B	
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Schematic modify Item and History :

B2-->B3

1. Power -

- A. Change PL11 from 4.7uH to 15uH
- B. Delete PJP5

2. Design issue -

- A. Correct part refence from 12 to U24
- B. Change C299 part number
- C. Add test points: U28, pins 1, 4, 17, 29, 36, and 37
- d. Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L
- e. RTC issue: VIA recommend to delete R216

1. DCON POWER -

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Schematic modify Item and History :

C1-->C2

1. Power -

A. PU6/PU7 (AOZ1021): correct the R/C of comp pin to 11K and 2.2nF

B. Change the PQ21 from CHDTC144U to ME1304AT3 (Vgs<1V)

page 27 C. Correct the +3.3VSUS to 3VPCU on PR69.1 and PR62 for prevent the +1.2V_GD glitch

D. Change the Q13 and PQ31 to AO3404 for power good glitch by +3.3V & 5V sequence issue on PU3

E. Add MAX1776 circuit for TPS62050 L/T time isn't enough.

F. Correct the +1.2V discharge circuit

page 26 G. modify the PU12.14 and connect to PQ44.3 for excessive power

page 25 H. Add R/C delay on PRE_MAIN_ON to control MAIN_ON for S3 issue and reserve the D42 between MAIN_ON and PRE_MAIN_ON 3 quickly +1.2V discharge

page 24 I. Correct the Q37.2 form WL_SW to WLAN_3.3V for WLAN power sequence

J. Change the C446 to 0.47uF for prevent the glitch of WLAN_3.3V

K. Change the Q40.1 from +3.3V to WLAN_3.3V to prevent the leakage of WLAN_3.3V

page 23 L. Pull high on U28.55 for un-used Low battery function

M. correct the R366 and R362 for EC_ID

page 21 N. SWAP the CON2.10 and CON.11

O. Add L/C on Q2.1 for DVDD_1.8V excessive noise.

page 20 P. For EMI request, change R384 to C370 & R386 to C25

Q. Change C8 to R126 for preventing no sound on speaker when S3/reboot resume.

F. Power team suggest:

1. Reserve PC123, PR164.

2. Short the PU8.2 & PU8.6 to GND for Vin_OK keep high

2. Design issue -

A. Correct part reference from 12 to U24

B. Change C299 part number

C. Add test points: U28, pins 1, 4, 17, 29, 36, and 37

d. Change U29 pin 37, 36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L

e. RTC issue: VIA recommend to delete R216

1. DCON POWER -

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Schematic modify Item and History :

C2-->C3

1. *Boot problems:*

PR31 : 22ohm -> 10ohm. (10 ohm is normal value.)

2. *Flash problems:*

Add pull-up resistor R396 (4.7k 0402).

3. *Very loud whining when connected to a solar panel*

Relpace PD22 to schottky diode and invert it (the cathode of PD22 connect to PR152/PC102).

PC102 - 0.47uF, 6V, 0402, Y7V

PR116 - 475K, 1%, 0402

PR117 - 28K, 1%, 0402

PR120 - 28K, 1%, 0402

PR125 - 2.2K, 5%, 0402

PR126 - 2.2K, 5%, 0402

PR144 - 330K, 1%, 0402

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Schematic modify Item and History :

C6-->C7

1. C3/C4 problems:

Page 05: Populate C299.

Page 06: Add C374 and C382 near to CPU

Page 30: PR176 and PR177 close to PU3

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<Title>		
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