CL1B Block Diagram

C3
2010-10-08

VTERM(+0.9V)
VTT(+1.05V)
+1.5VSUS
+1.5V
+1.8VMEM
+1.8V
+2.5V
3VPCU
+3.3V
+3.3VSUS
LCD_3.3V
LCD_5V
+5V

C7-M (ULV)

VCORE:+1.196 ~ +0.748
VCCP:+1.05V
VCCA:+1.8V or +1.5V

VID[0:6] → CPU VCORE

+/- CPU_CLK
+/- HCLK → Clock Gengerator ICS9UM7002

V4 BUS

Frame Buffer → DCON → 7" LCD

VX855(U)

VTT:VCCP (+1.05V)
VCC15:+1.5V or +1.2V
VCC33:+3.3V
VCCMEM:+1.8V
VSUS15:+1.5VSUS
VSUS33:+3.3VSUS

CHA → DDRII 1GB

SDIO I/F → MICRO SD

VIP I/F → Camera

SDIO I/F → WLAN Conn. → WLAN Module

WLAN Conn. → Card Reader SD Card SLOT

USB → USB PORT X3

HD Audio → HDA CODEC CX20582 → Int. SPK, Audio Jack, Int. Mic

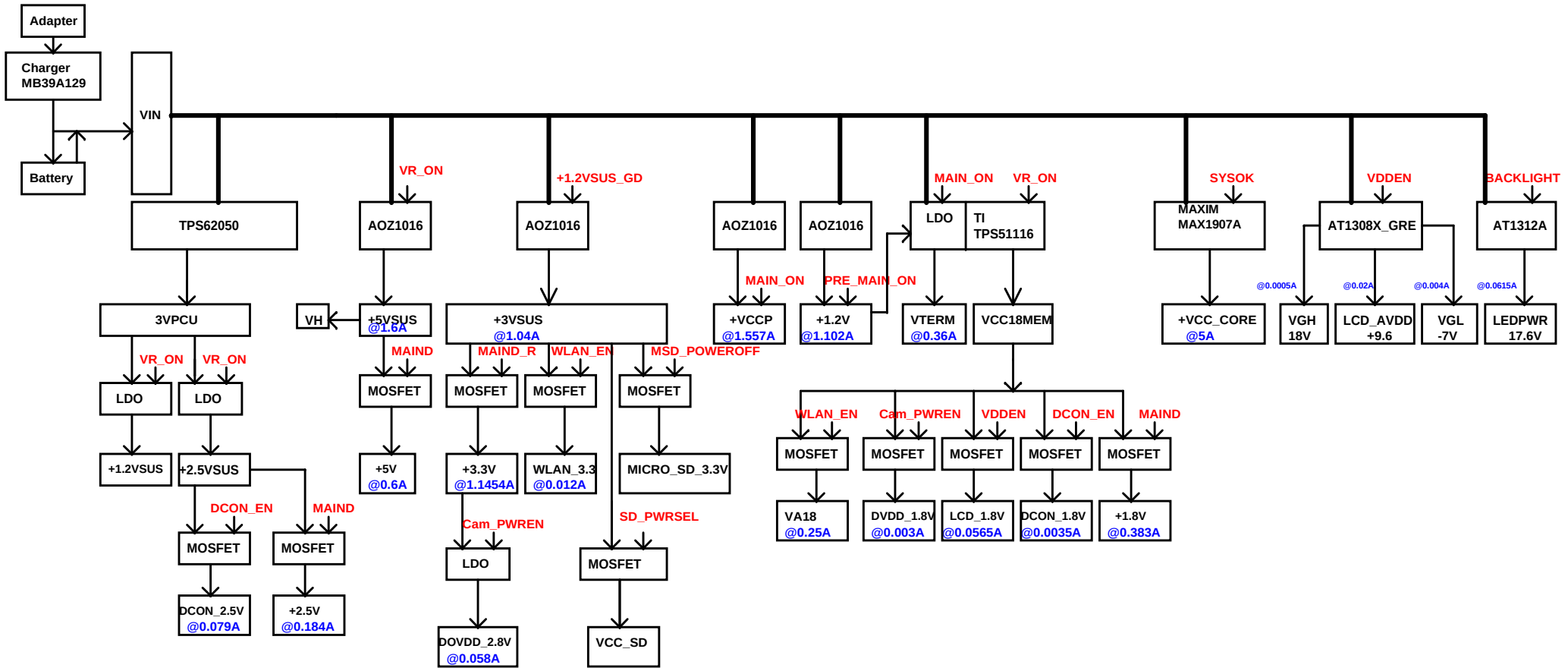
LPC BUS → EC KB3700 → SPI Flash

EC KB3700 → Int. KB, T/P, Battery → Charger

Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	BLOCK DIAGRAM	3B

Date: Friday, October 08, 2010 Sheet 1 of 38

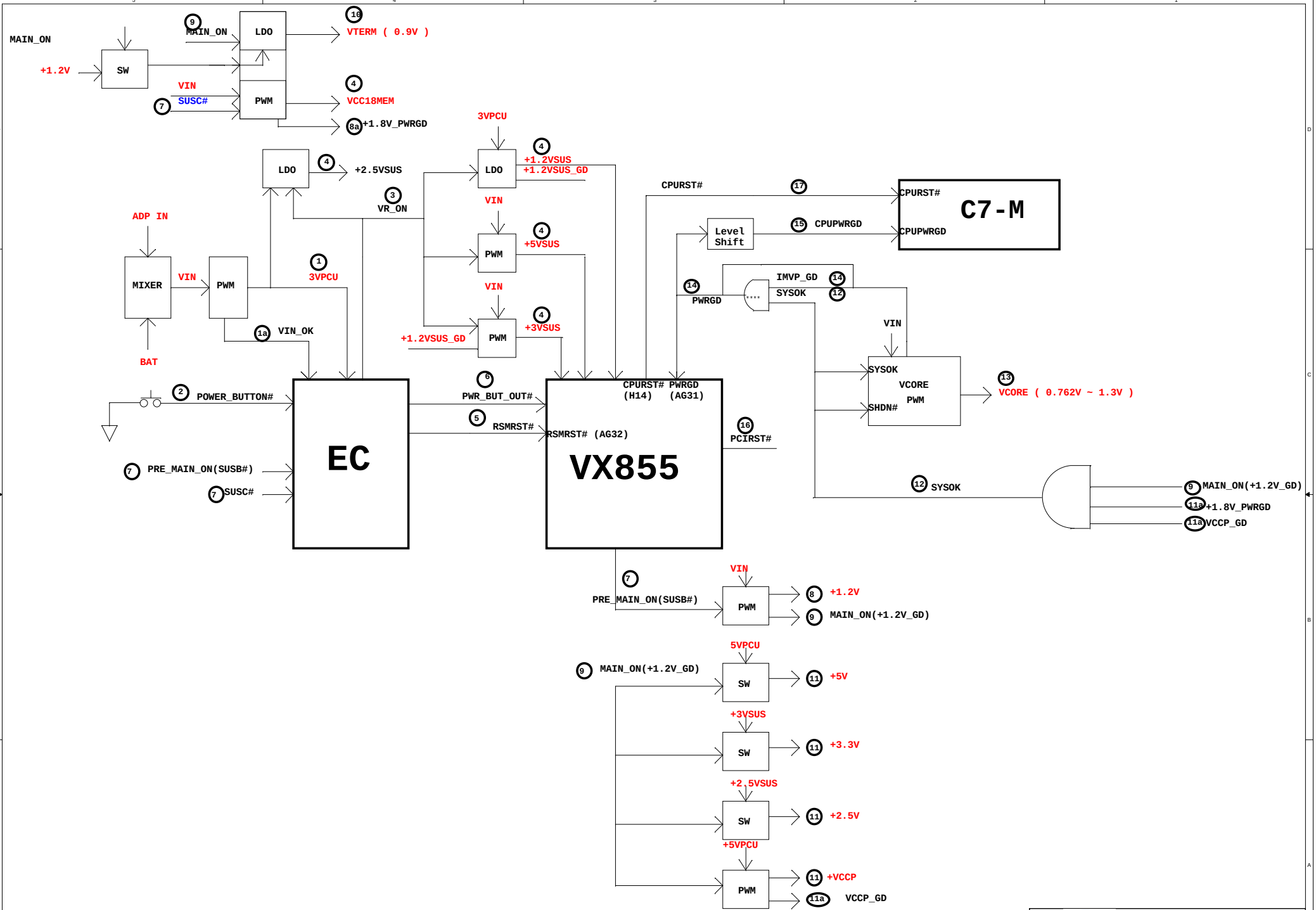


Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	POWER MANGER DIAGRAM	3B

Date: Friday, October 08, 2010 Sheet 2 of 38

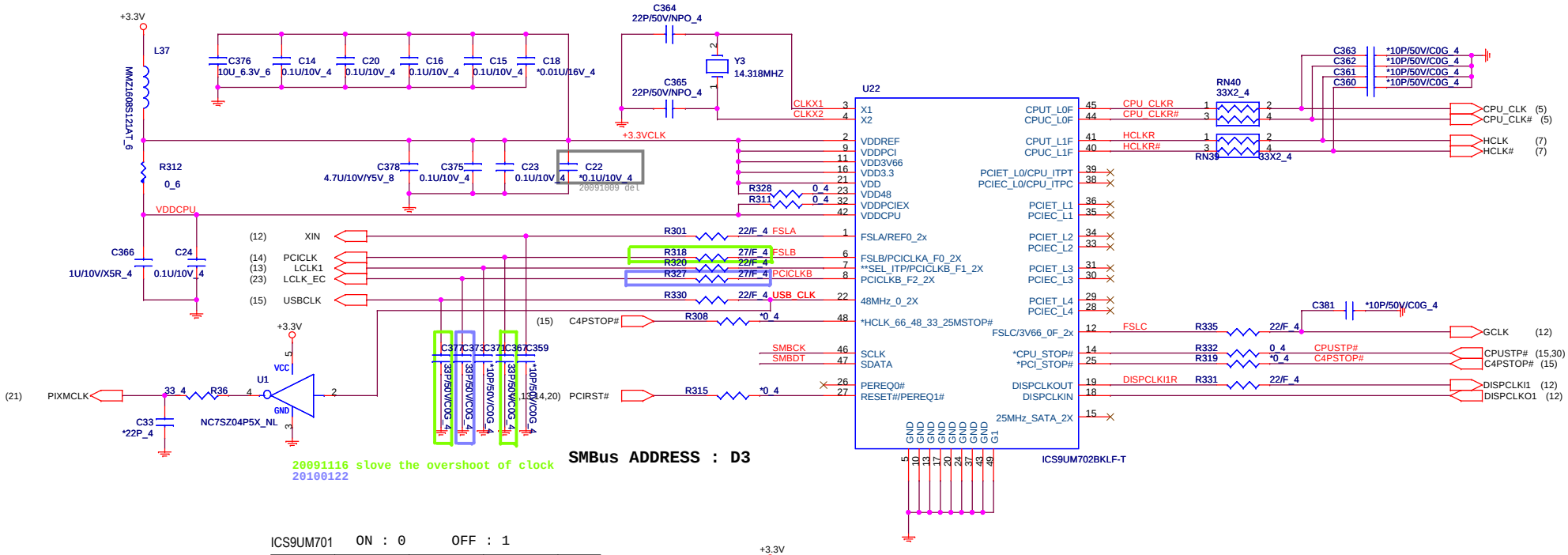


Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	Power Sequency	3B

Date: Friday, October 08, 2010 Sheet 3 of 38

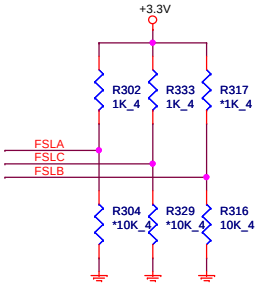


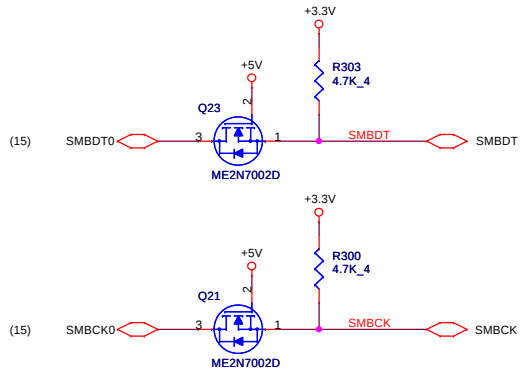
20091116 slove the overshoot of clock
20100122

SMBus ADDRESS : D3

ICS9UM701 ON : 0 OFF : 1

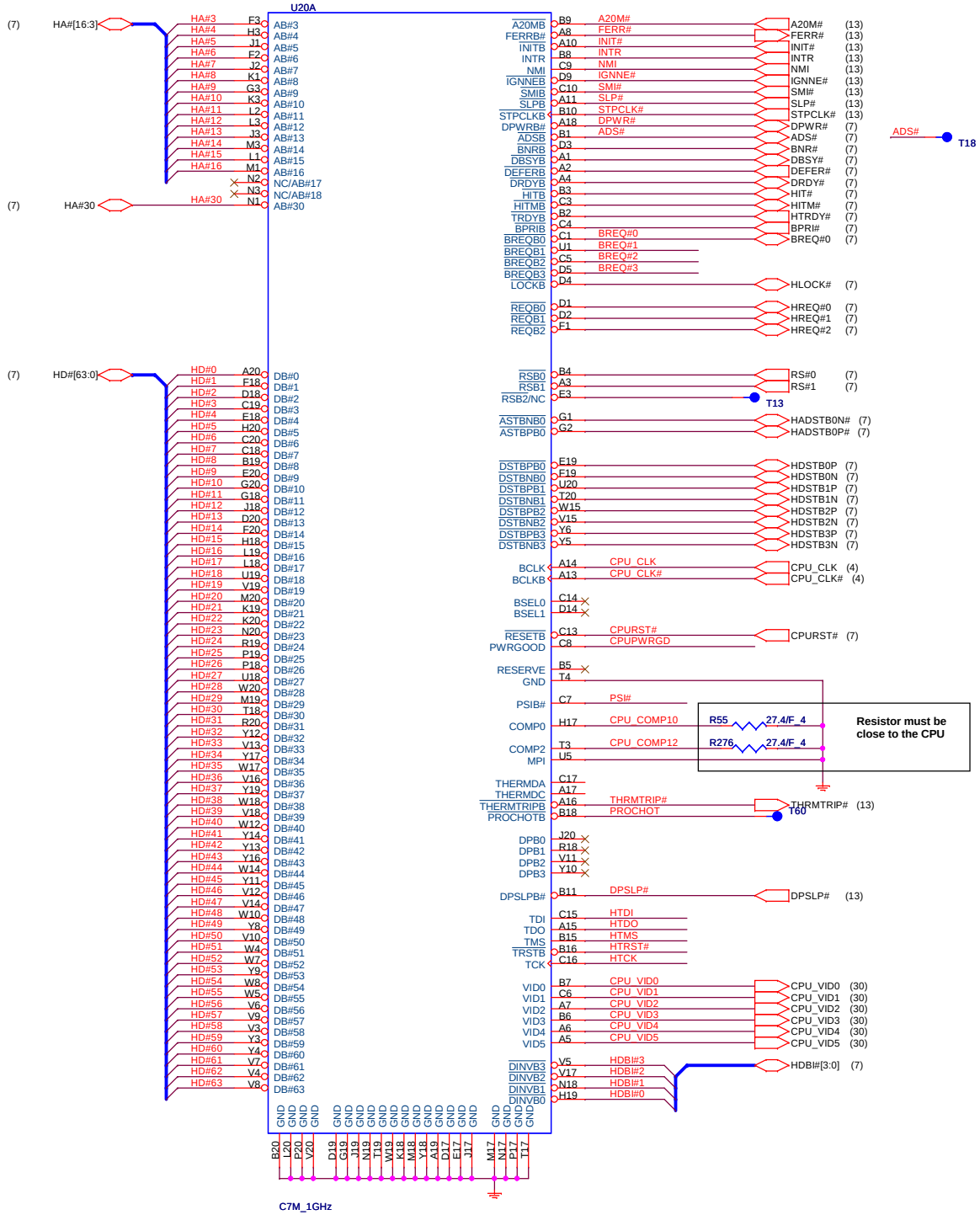
3	2	1		
FSLA	FSLC	FSLB	CPU	PCI
0	0	0	266.66	33
1	0	0	133.33	33
0	0	1	200	33
1	0	1	166.66	33
0	1	0	333.33	33
1	**1**	**0**	**100**	33
0	1	1	400	33
1	**1**	**1**	**200**	33

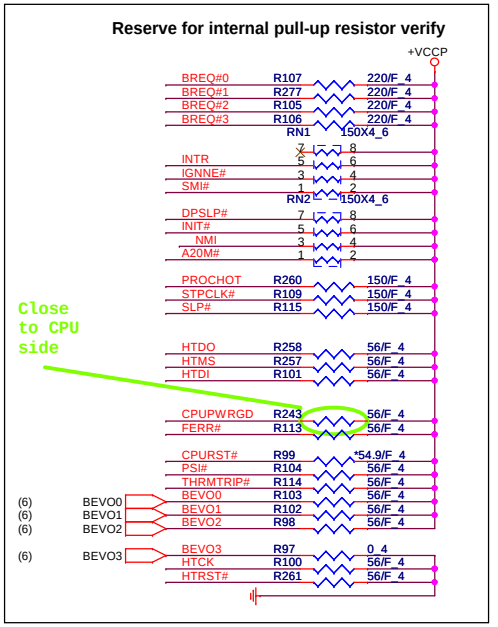


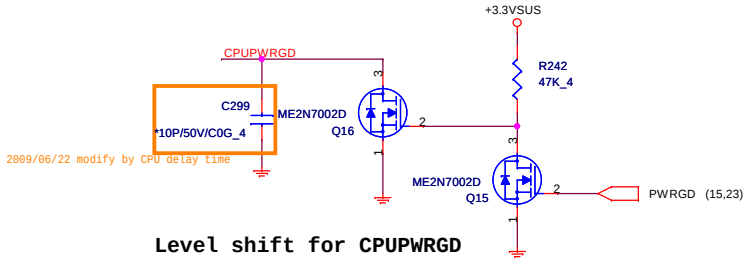


Quanta Computer Inc.
PROJECT : CL1B

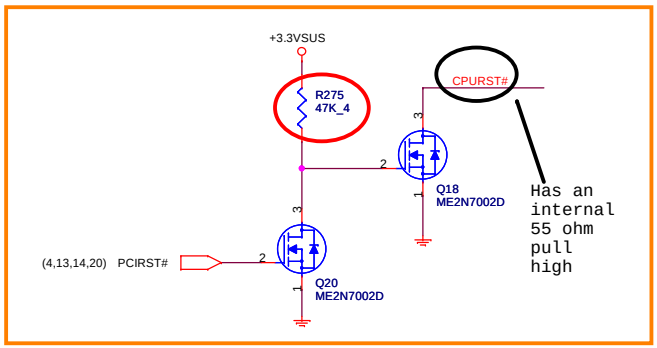
Size	Document Number	Rev
	CLOCK GENERATOR	3B
Date: Friday, October 08, 2010	Sheet 4 of 38	



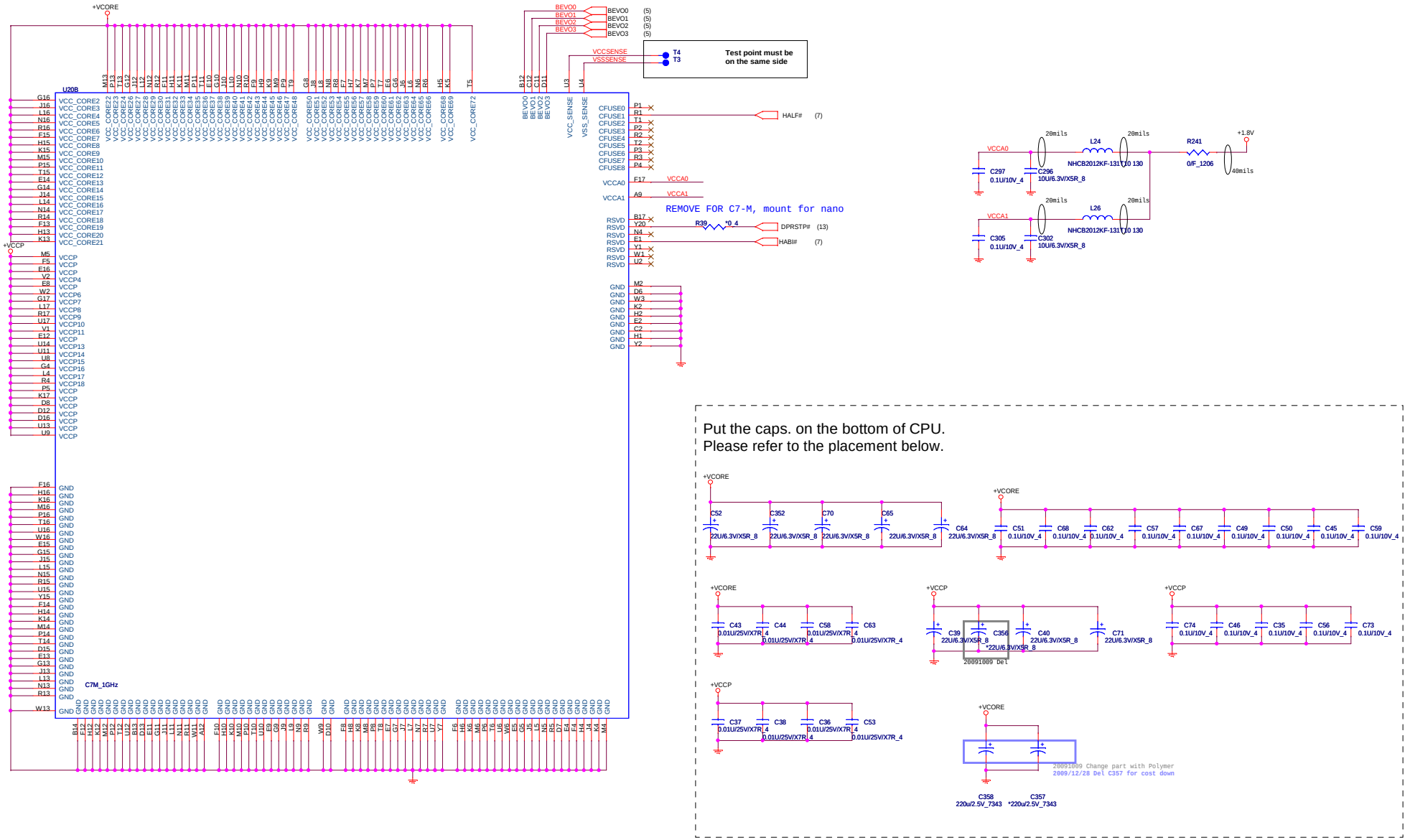




Level shift for CPUPWRGD



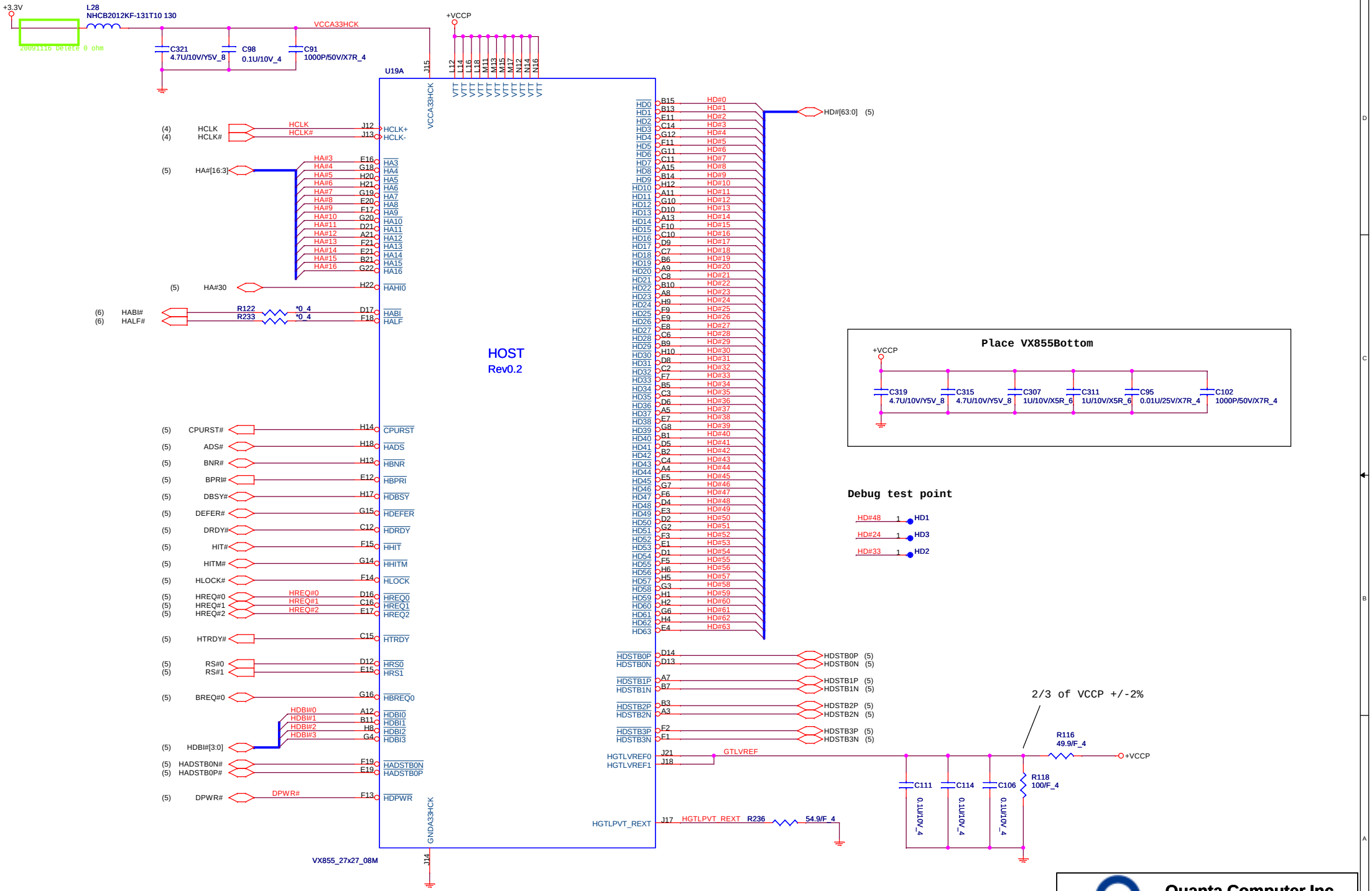
Quanta Computer Inc.			
PROJECT : CL1B			
Size	Document Number		Rev
	CPU C7M V4BUS		3B
Date:	Friday, October 08, 2010	Sheet 5 of 38	



Put the caps. on the bottom of CPU.
Please refer to the placement below.

Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	CPU C7M POWER&GND	3B
Date: Friday, October 08, 2010	Sheet 6 of 38	

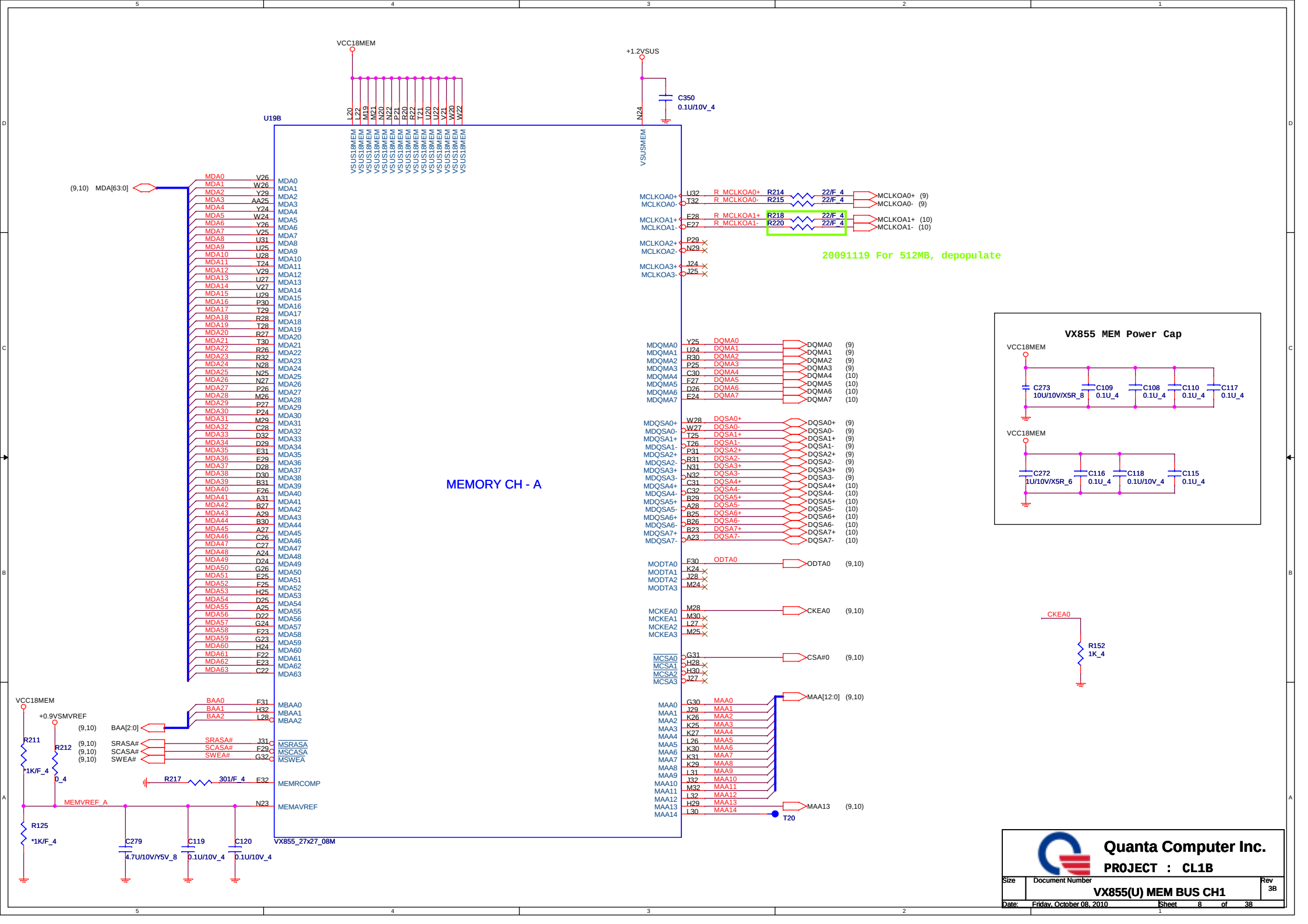


Quanta Computer Inc.

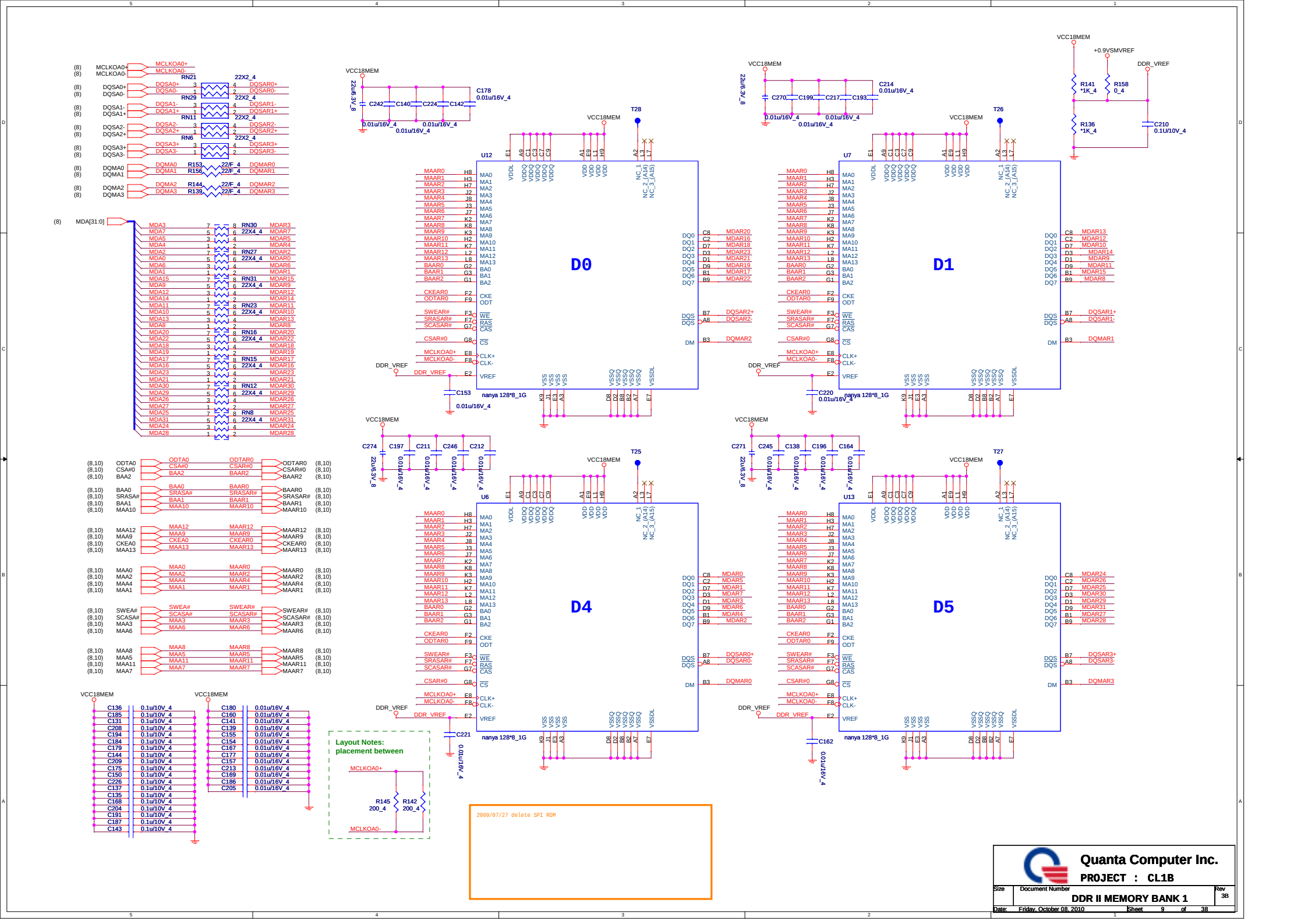
PROJECT : CL1B

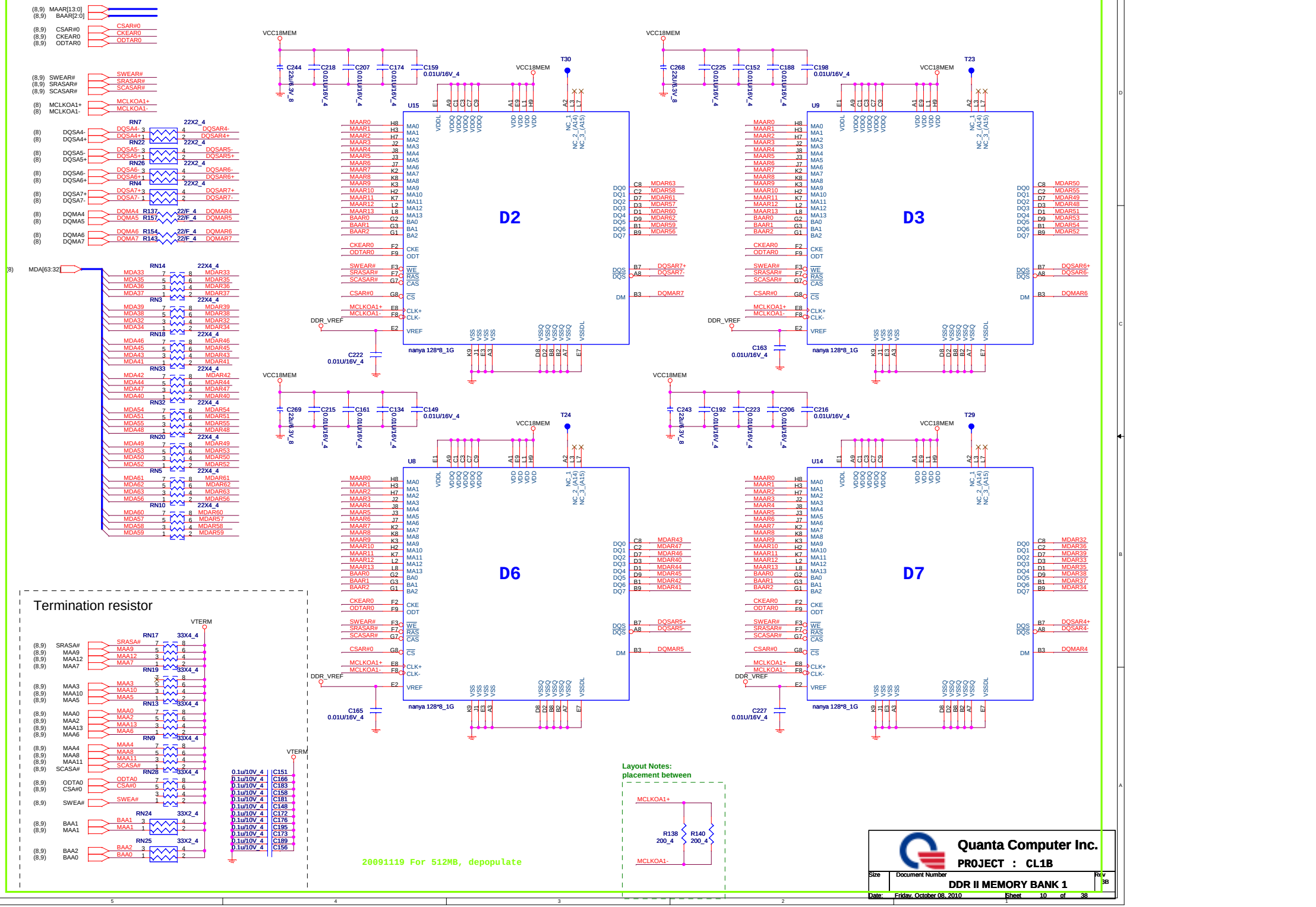
Size	Document Number	Rev
	VX855(U) HOST BUS	3B

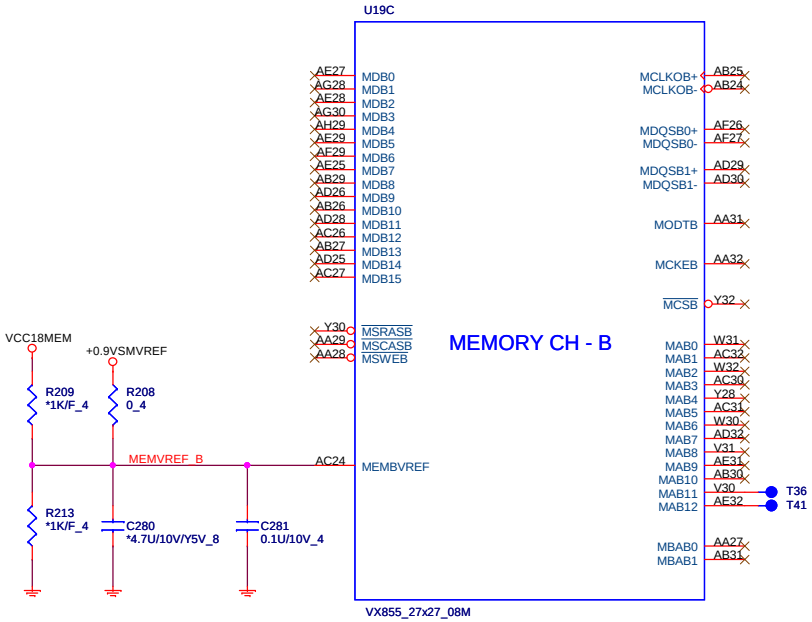
Date: Friday, October 08, 2010 Sheet 7 of 38



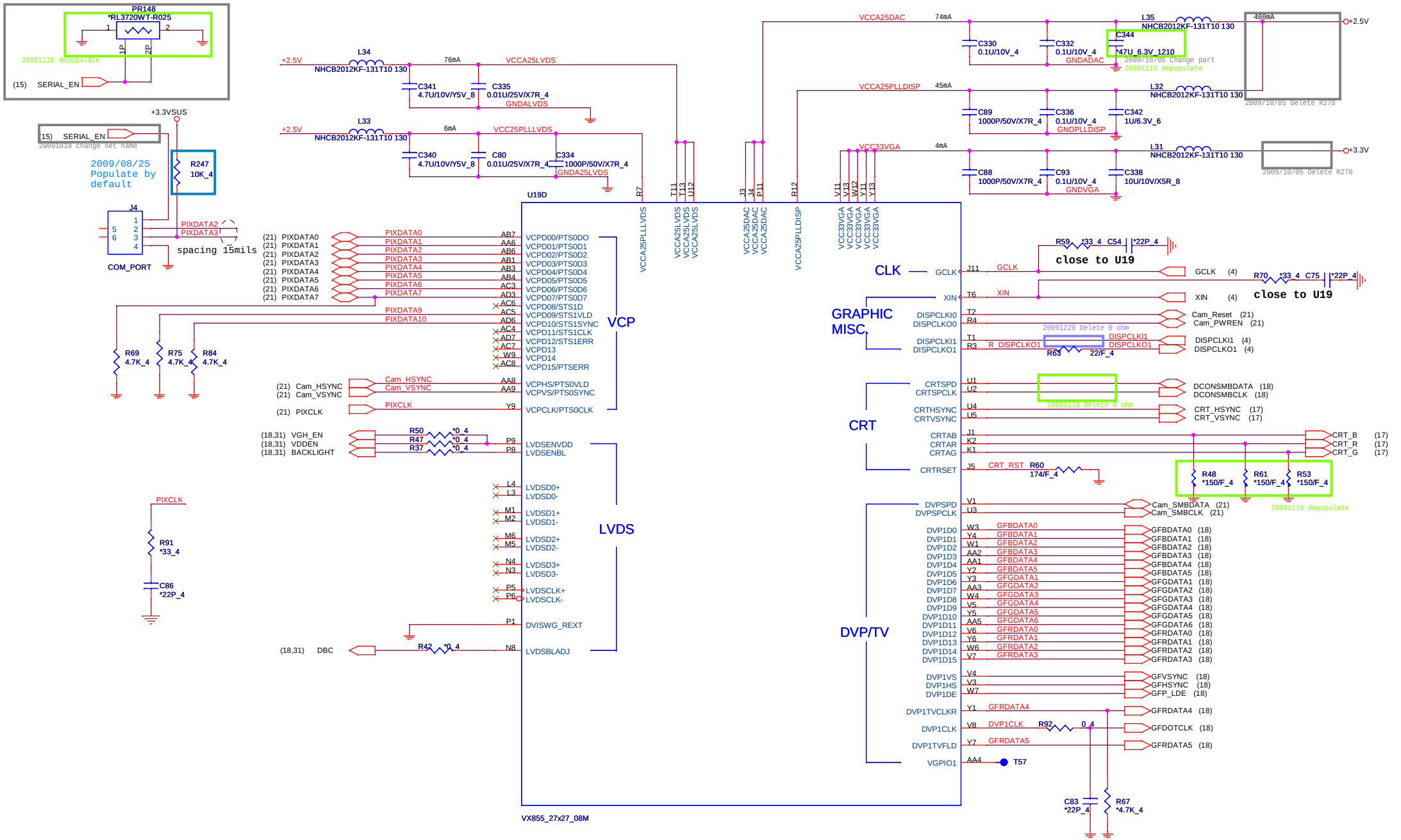
Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number	Rev
	VX855(U) MEM BUS CH1	3B
Date: Friday, October 08, 2010	Sheet 8 of 38	


D0
D1
D4
D5
U12
U7
U6
U13
T28
T26
T25
T27
nanya 128*8_1G
VCC18MEM
DDR_VREF
+0.9VSMVREF
MCLKOA0+
MCLKOA0-
MDA[31:0]
Layout Notes:
placement between
2009/07/27 delete SPI ROM
Quanta Computer Inc.
PROJECT : CL1B
DDR II MEMORY BANK 1
Size
Document Number
Rev
3B
Date: Friday, October 08, 2010
Sheet 9 of 38


(8,9) MAAR[13:0]
(8,9) BAAR[2:0]
CSAR#0
CKEAR0
ODTAR0
(8,9) CSAR#0
(8,9) CKEAR0
(8,9) ODTAR0
(8,9) SWEAR#
(8,9) SRASAR#
(8,9) SCASAR#
SWEAR#
SRASAR#
SCASAR#
(8) MCLKOA1+
(8) MCLKOA1-
MCLKOA1+
MCLKOA1-
RN7 22X2_4
RN22 22X2_4
RN26 22X2_4
RN4 22X2_4
(8) DQSA4-
(8) DQSA4+
(8) DQSA5-
(8) DQSA5+
(8) DQSA6-
(8) DQSA6+
(8) DQSA7+
(8) DQSA7-
DQSAR4-
DQSAR4+
DQSAR5-
DQSAR5+
DQSAR6-
DQSAR6+
DQSAR7+
DQSAR7-
(8) DQMA4
(8) DQMA5
(8) DQMA6
(8) DQMA7
R137 22/F_4
R157 22/F_4
R154 22/F_4
R143 22/F_4
DQMAR4
DQMAR5
DQMAR6
DQMAR7
(8) MDA[63:32]
RN14 22X4_4
RN3 22X4_4
RN18 22X4_4
RN33 22X4_4
RN32 22X4_4
RN20 22X4_4
RN5 22X4_4
RN10 22X4_4
MDA33 MDA35 MDA36 MDA37 MDAR33 MDAR35 MDAR36 MDAR37
MDA39 MDA38 MDA32 MDA34 MDAR39 MDAR38 MDAR32 MDAR34
MDA46 MDA45 MDA43 MDA41 MDAR46 MDAR45 MDAR43 MDAR41
MDA42 MDA44 MDA47 MDA40 MDAR42 MDAR44 MDAR47 MDAR40
MDA54 MDA51 MDA55 MDA48 MDAR54 MDAR51 MDAR55 MDAR48
MDA49 MDA53 MDA50 MDA52 MDAR49 MDAR53 MDAR50 MDAR52
MDA61 MDA62 MDA63 MDA56 MDAR61 MDAR62 MDAR63 MDAR56
MDA60 MDA57 MDA58 MDA59 MDAR60 MDAR57 MDAR58 MDAR59
Termination resistor
VTERM
RN17 33X4_4
RN19 33X4_4
RN13 33X4_4
RN9 33X4_4
RN28 33X4_4
RN24 33X2_4
RN25 33X2_4
(8,9) SRASA#
(8,9) MAA9
(8,9) MAA12
(8,9) MAA7
(8,9) MAA3
(8,9) MAA10
(8,9) MAA5
(8,9) MAA0
(8,9) MAA2
(8,9) MAA13
(8,9) MAA6
(8,9) MAA4
(8,9) MAA8
(8,9) MAA11
(8,9) SCASA#
(8,9) ODTA0
(8,9) CSA#0
(8,9) SWEA#
(8,9) BAA1
(8,9) MAA1
(8,9) BAA2
(8,9) BAA0
0.1u/10V_4 C151 C166 C183 C158 C181 C148 C172 C176 C195 C173 C189 C156
VCC18MEM
C244 C218 C207 C174 C159 0.01U/16V_4
C268 C225 C152 C188 C198 0.01U/16V_4
C269 C215 C161 C134 C149 0.01U/16V_4
C243 C192 C223 C206 C216 0.01U/16V_4
22u/6.3V_8
T30
T23
T24
T29
U15
U9
U8
U14
D2
D3
D6
D7
nanya 128*8_1G
DDR_VREF
C222 0.01U/16V_4
C163 0.01U/16V_4
C165 0.01U/16V_4
C227 0.01U/16V_4
Layout Notes:
placement between
MCLKOA1+
MCLKOA1-
R138 200_4
R140 200_4
20091119 For 512MB, depopulate
Quanta Computer Inc.
PROJECT : CL1B
Size
Document Number
DDR II MEMORY BANK 1
Rev
3B
Date: Friday, October 08, 2010
Sheet 10 of 38



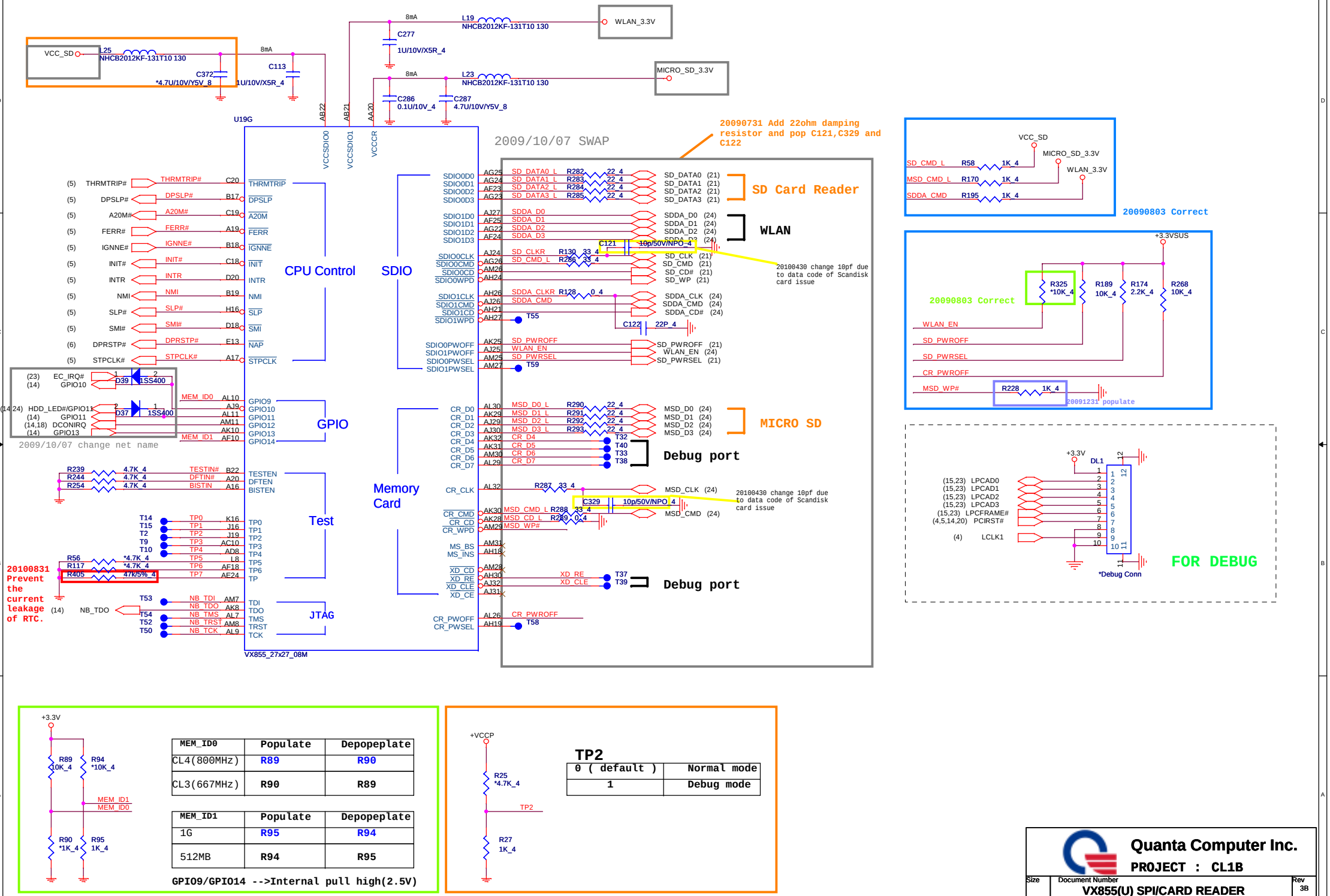
Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number: VX855(U) MEM BUS CH2 & PCIE	Rev: 3B
Date: Friday, October 08, 2010	Sheet 11 of 38	



Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) VIDEO BUS	3B
Date: Friday, October 08, 2010	Sheet 12 of 38	



MEM_ID0	Populate	Depopeplate
CL4(800MHz)	R89	R90
CL3(667MHz)	R90	R89

MEM_ID1	Populate	Depopeplate
1G	R95	R94
512MB	R94	R95

GPIO9/GPIO14 -->Internal pull high(2.5V)

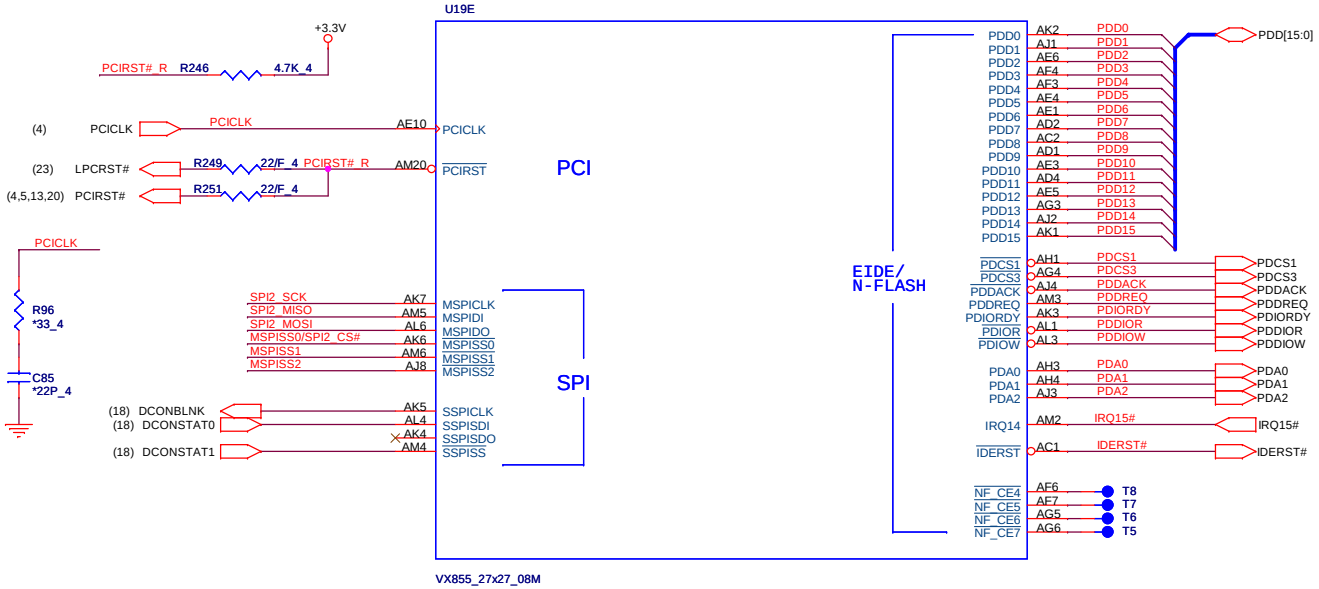
TP2

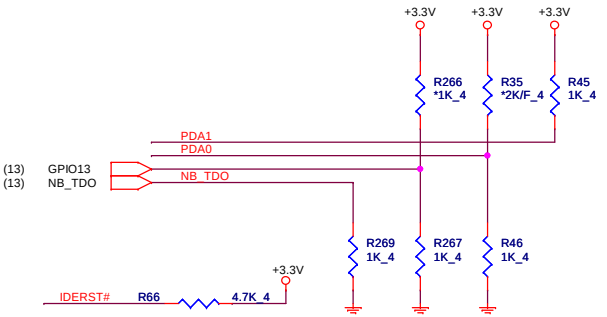
0 (default)	Normal mode
1	Debug mode

Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) SPI/CARD READER	3B

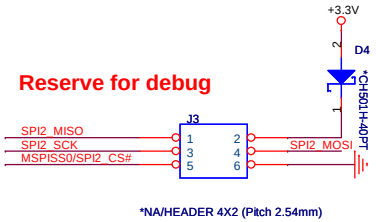
Date: Friday, October 08, 2010 Sheet 13 of 38

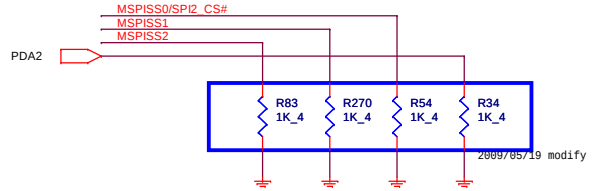


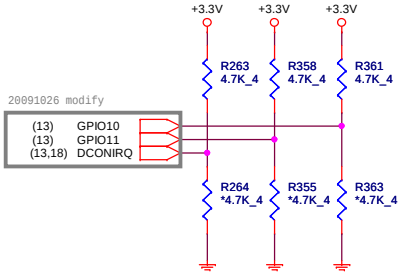


NB Strapping

Pin	Function	Pull Low	Pull High
PDA1	PLL OK source select	from NB PLL	from SB Logic*
PDA0	IOQ depth	12 *	1
GPIO13	GTL pull up	Enable *	Disable
NB_TDO	Debug Link enable	XD Mode*	Debug Link

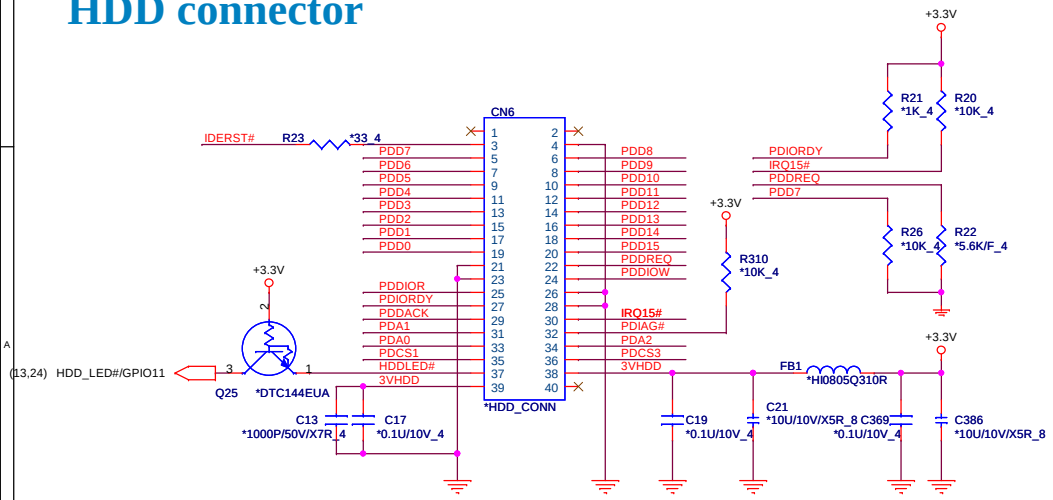






2009/10/01 don't populate

HDD connector



SB Strapping

Pin	0:LOW 1:High	Function
MSPISS1/ MSPISS0	00*	IDE
	01	NFC
	10	CE ATA
MSPISS2	0: SPI/LPC *	NFC ROM Select
	1: NFC ROM	
PDA2	0: Disable *	PCI Master Mode Enable
	1: Enable	

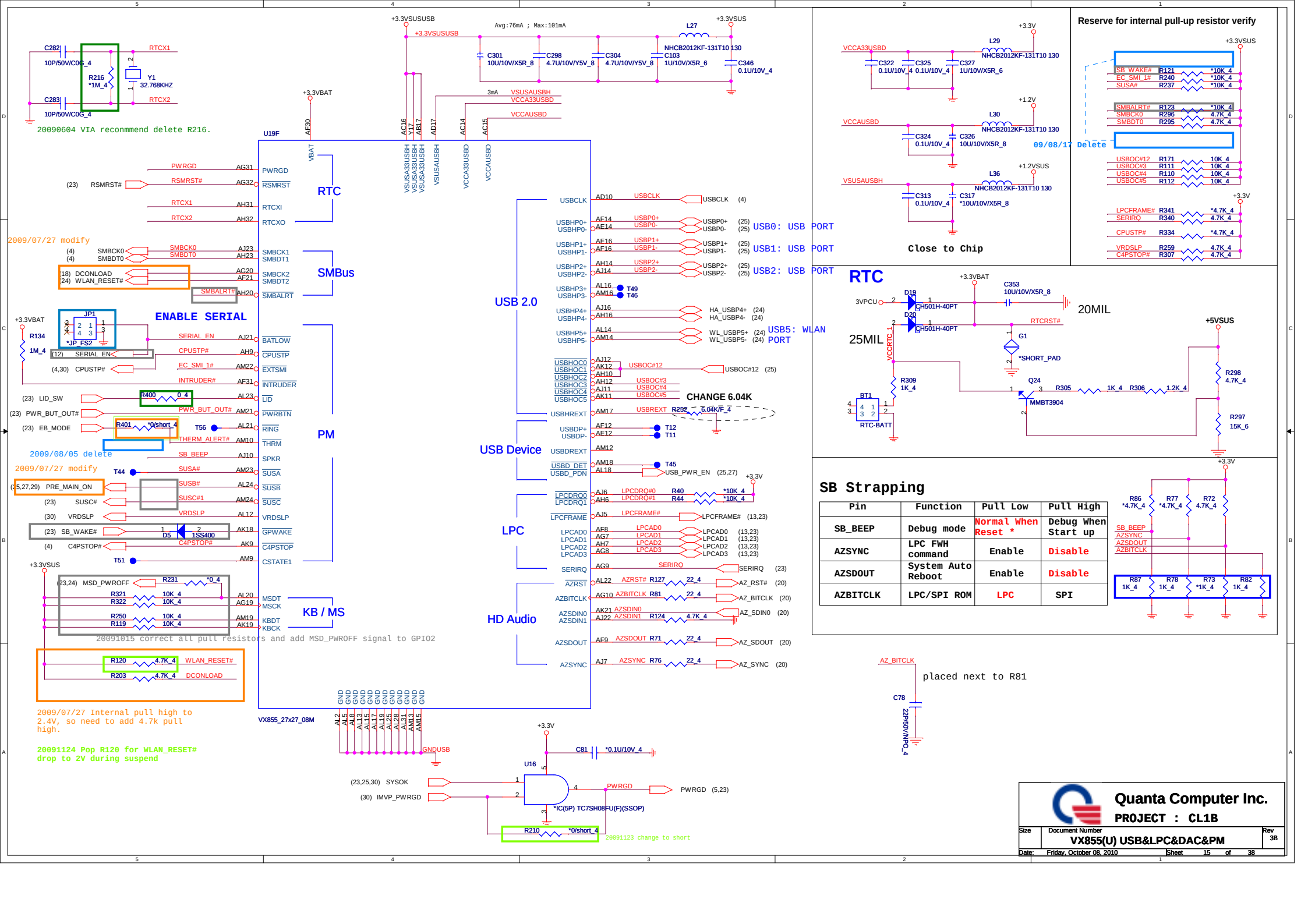
NB Strapping

Pin	0:Low 1:High	FSB Freq.
GPIO12/ GPIO11/ GPIO10	000	100Mhz
	001	133Mhz
	010	200Mhz
	011	266Mhz
	111 *	Auto Mode

Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) PCI&PATA&SATA BUS	3B
Date: Friday, October 08, 2010	Sheet 14 of 38	


C282 10P/50V/C0G_4
C283 10P/50V/C0G_4
R216 *1M_4
Y1 32.768KHZ
RTCX1
RTCX2
20090604 VIA reconmmend delete R216.
+3.3VSUSUSB
Avg:76mA ; Max:101mA
L27
NHCB2012KF-131T10 130
C301 10U/10V/X5R_8
C298 4.7U/10V/Y5V_8
C304 4.7U/10V/Y5V_8
C103 1U/10V/X5R_6
C346 0.1U/10V_4
+3.3VSUS
+3.3VBAT
3mA
VSUSAUSBH
VCCA33USBD
VCCAUSBD
U19F
VBAT
RTC
PWRGD
RSMRST#
RTCXI
RTCXO
SMBus
SMBCK0
SMBDT0
SMBCK1
SMBDT1
SMBCK2
SMBDT2
SMBALRT#
DCONLOAD
WLAN_RESET#
ENABLE SERIAL
JP1
*JP_FS2
SERIAL_EN
CPUSTP#
EC_SMI_1#
INTRUDER#
LID_SW
PWR_BUT_OUT#
EB_MODE
THERM_ALERT#
SB_BEEP
SUSA#
SUSB#
SUSC#
VRDSLP
SB_WAKE#
C4PSTOP#
PRE_MAIN_ON
MSD_PWROFF
PM
KB / MS
BATLOW
CPUSTP
EXTSMI
INTRUDER
LID
PWRBTN
RING
THRM
SPKR
SUSA
SUSB
SUSC
VRDSLP
GPWAKE
C4PSTOP
CSTATE1
MSDT
MSCK
KBDT
KBCK
2009/07/27 modify
2009/08/05 delete
2009/07/27 modify
20091015 correct all pull resistors and add MSD_PWROFF signal to GPIO2
2009/07/27 Internal pull high to 2.4V, so need to add 4.7k pull high.
20091124 Pop R120 for WLAN_RESET# drop to 2V during suspend
VX855_27x27_08M
USB 2.0
USB Device
LPC
HD Audio
USBCLK
USBP0+
USBP0-
USBP1+
USBP1-
USBP2+
USBP2-
USB0: USB PORT
USB1: USB PORT
USB2: USB PORT
USB5: WLAN PORT
HA_USBP4+
HA_USBP4-
WL_USBP5+
WL_USBP5-
USBOC#12
USBOC#3
USBOC#4
USBOC#5
CHANGE 6.04K
USBREXT
USBDP+
USBDP-
USBDREXT
USB_DET
USB_PDN
USB_PWR_EN
LPCDRQ0
LPCDRQ1
LPCFRAME#
LPCAD0
LPCAD1
LPCAD2
LPCAD3
SERIRQ
AZRST#
AZBITCLK
AZSDIN0
AZSDIN1
AZSDOUT
AZSYNC
AZ_RST#
AZ_BITCLK
AZ_SDIN0
AZ_SDOUT
AZ_SYNC
GNDUSB
U16
*IC(5P) TC7SH08FU(F)(SSOP)
SYSOK
IMVP_PWRGD
PWRGD
C81 *0.1U/10V_4
R210 *0/short_4
20091123 change to short
+3.3V
VCCA33USBD
VCCAUSBD
VSUSAUSBH
L29
L30
L36
NHCB2012KF-131T10 130
+1.2V
+1.2VSUS
C322 0.1U/10V_4
C325 0.1U/10V_4
C327 1U/10V/X5R_6
C324 0.1U/10V_4
C326 10U/10V/X5R_8
C313 0.1U/10V_4
C317 *10U/10V/X5R_8
Close to Chip
Reserve for internal pull-up resistor verify
09/08/17 Delete
SB_WAKE# R121 *10K_4
EC_SMI_1# R240 *10K_4
SUSA# R237 *10K_4
SMBALRT# R123 *10K_4
SMBCK0 R296 4.7K_4
SMBDT0 R295 4.7K_4
USBOC#12 R171 10K_4
USBOC#3 R111 10K_4
USBOC#4 R110 10K_4
USBOC#5 R112 10K_4
LPCFRAME# R341 *4.7K_4
SERIRQ R340 4.7K_4
CPUSTP# R334 *4.7K_4
VRDSLP R259 4.7K_4
C4PSTOP# R307 4.7K_4
RTC
3VPCU
D19 CH501H-40PT
D20 CH501H-40PT
C353 10U/10V/X5R_8
20MIL
25MIL
VCCRTC_1
RTCRST#
G1
*SHORT_PAD
+5VSUS
R309 1K_4
BT1
RTC-BATT
Q24
MMBT3904
R305 1K_4
R306 1.2K_4
R298 4.7K_4
R297 15K_6
SB Strapping
Pin | Function | Pull Low | Pull High
SB_BEEP | Debug mode | Normal When Reset * | Debug When Start up
AZSYNC | LPC FWH command | Enable | Disable
AZSDOUT | System Auto Reboot | Enable | Disable
AZBITCLK | LPC/SPI ROM | LPC | SPI
R86 *4.7K_4
R77 *4.7K_4
R72 4.7K_4
R87 1K_4
R78 1K_4
R73 *1K_4
R82 1K_4
AZ_BITCLK
placed next to R81
C78 22P/50V/NPO_4
Quanta Computer Inc.
PROJECT : CL1B
Size
Document Number
VX855(U) USB&LPC&DAC&PM
Rev 3B
Date: Friday, October 08, 2010
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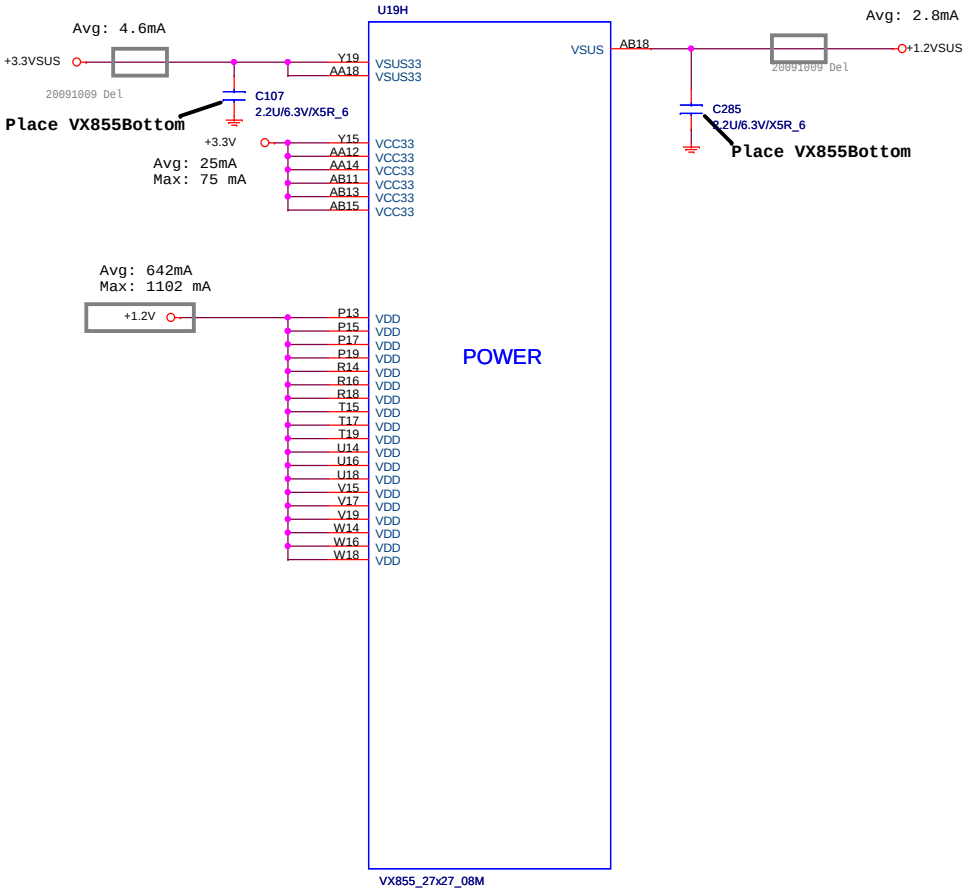
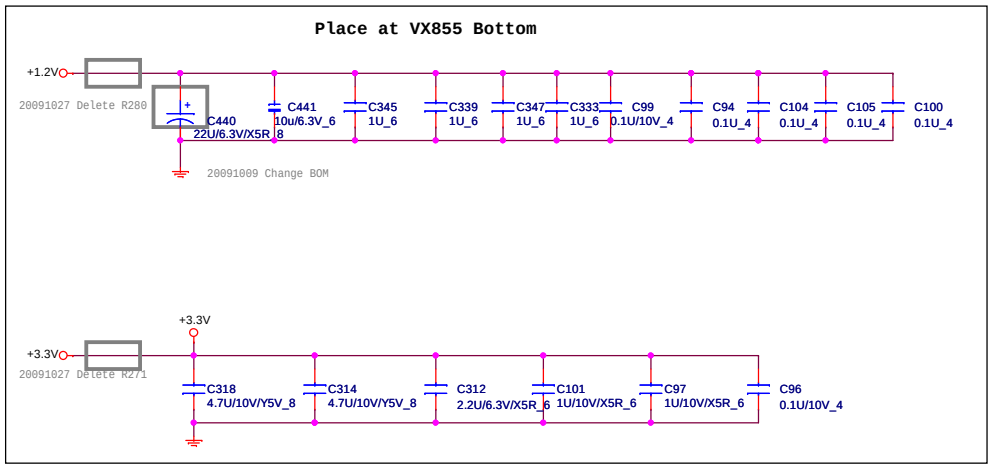
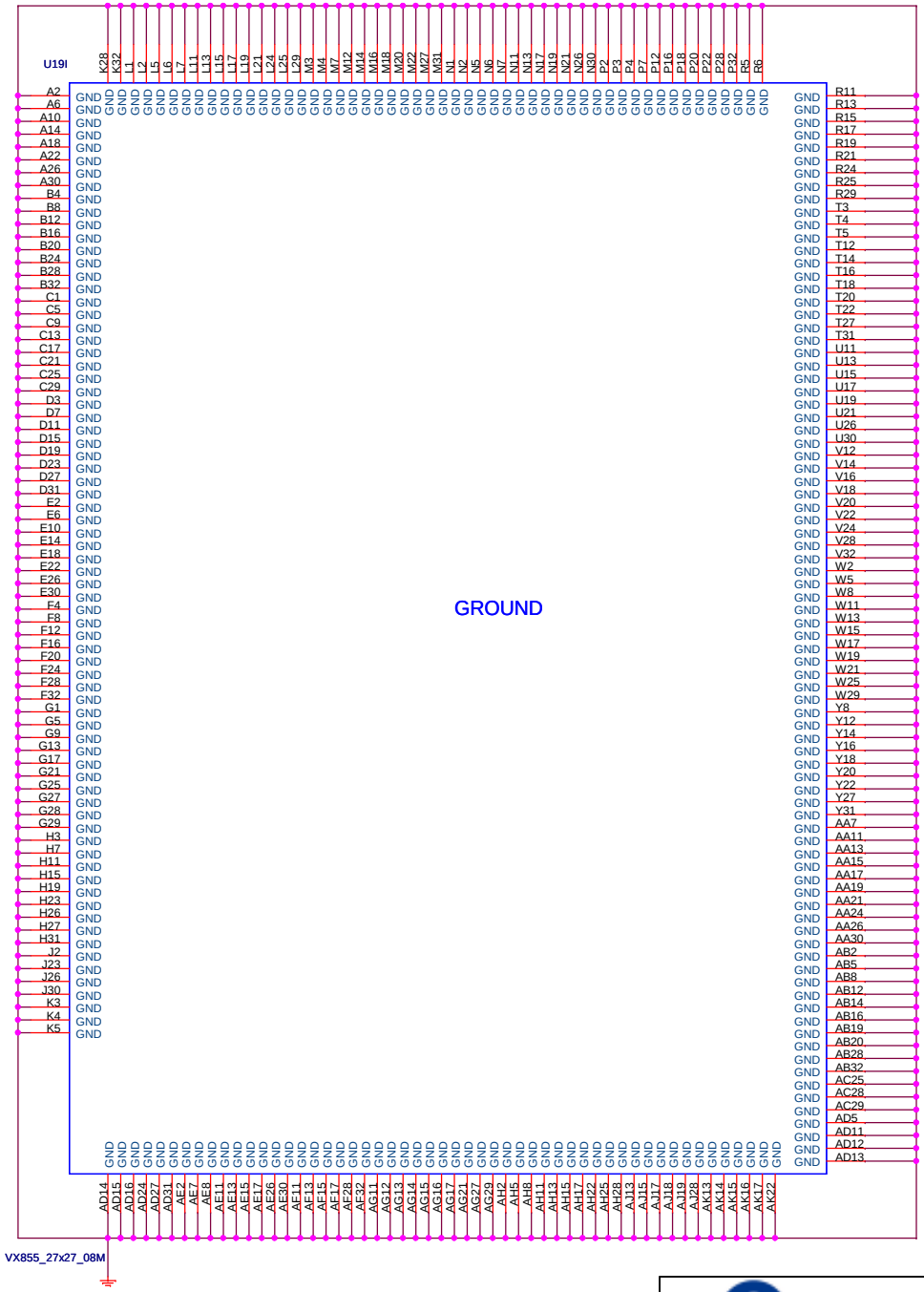




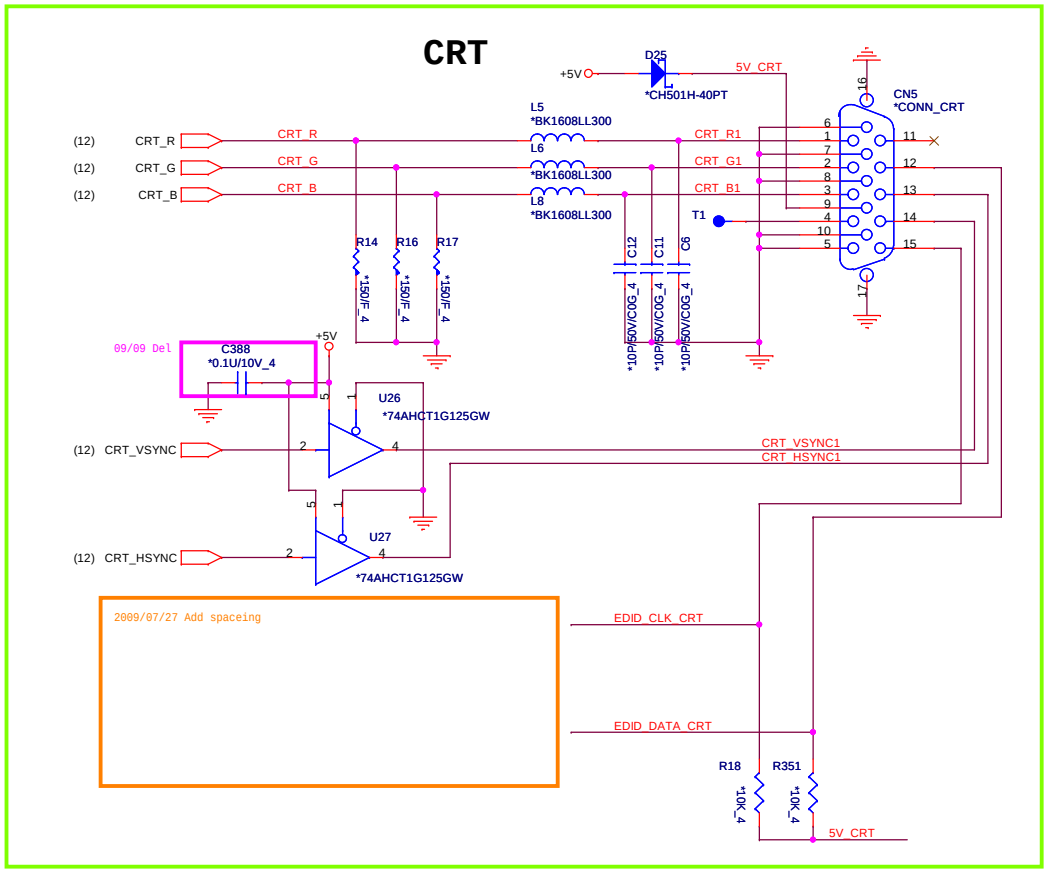


Quanta Computer Inc.

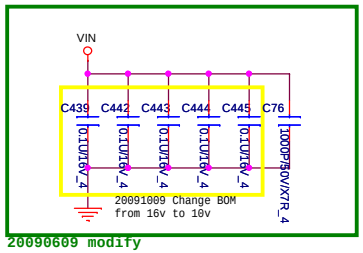
PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) POWER&GND	3B
Date: Friday, October 08, 2010	Sheet 16 of 38	

CRT

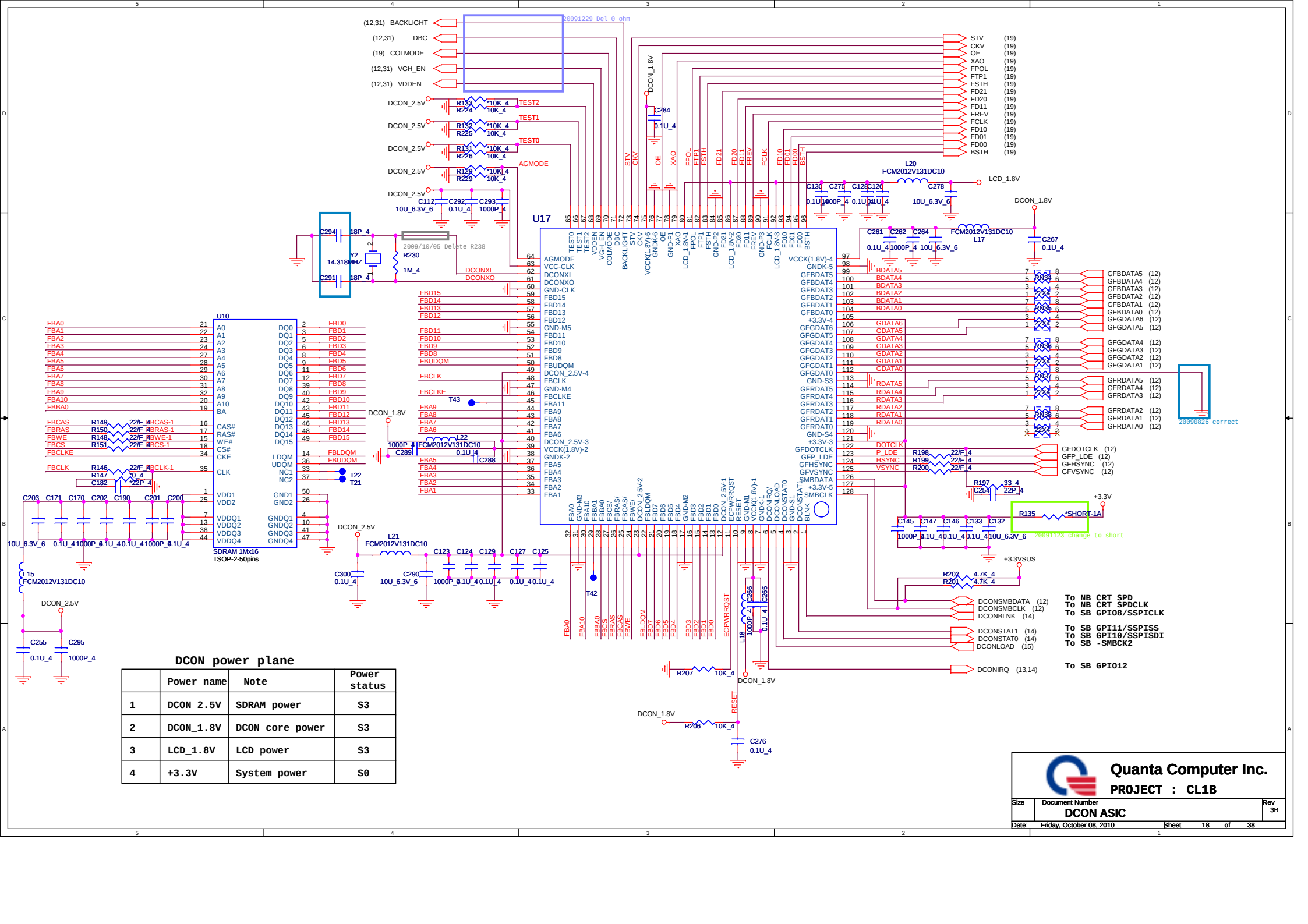


EMI



20090609 modify

Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number: CRT	Rev: 3B
Date: Friday, October 08, 2010	Sheet 17 of 38	



DCON power plane

	Power name	Note	Power status
1	DCON_2.5V	SDRAM power	S3
2	DCON_1.8V	DCON core power	S3
3	LCD_1.8V	LCD power	S3
4	+3.3V	System power	S0

Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	DCON ASIC	3B

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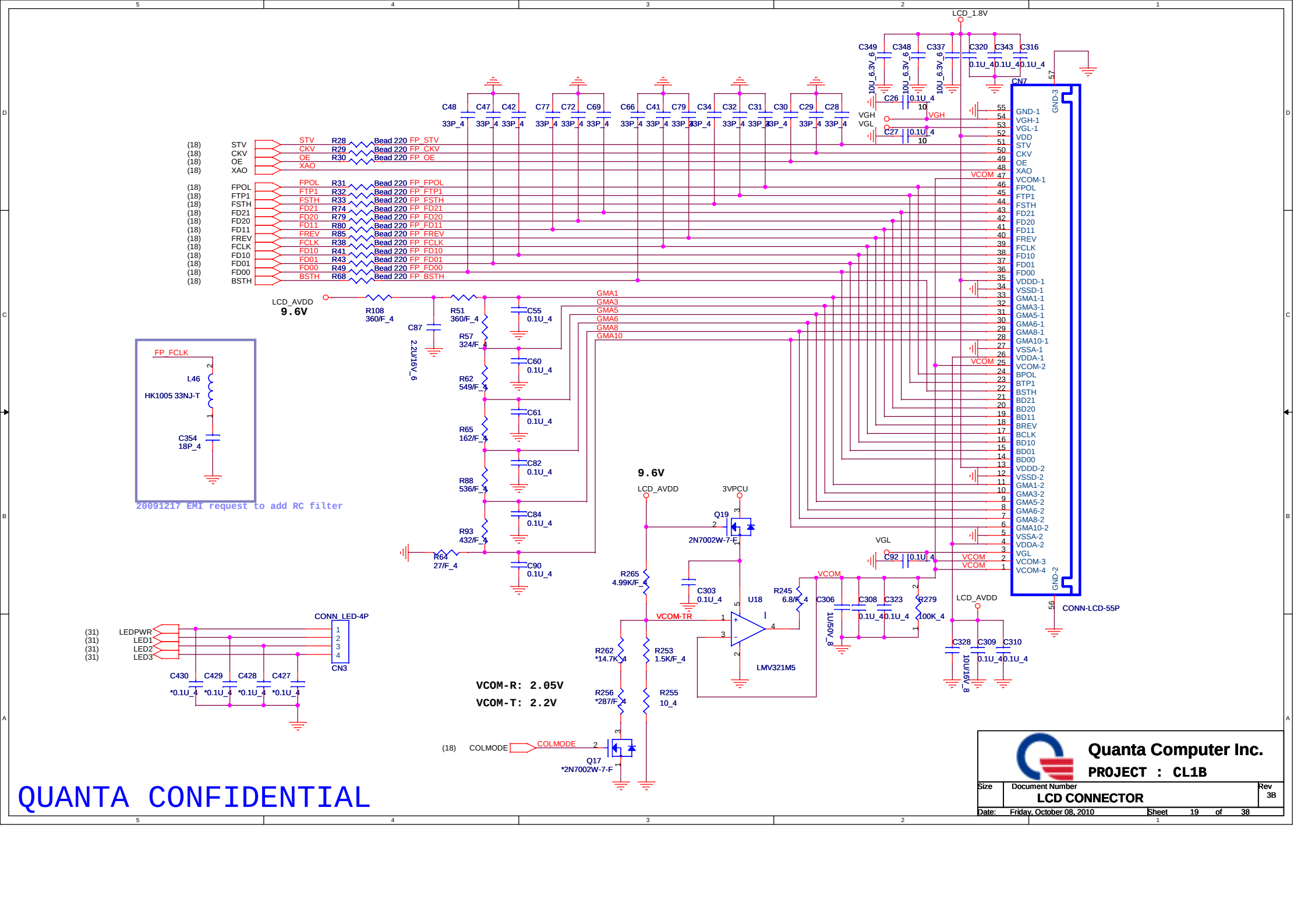

QUANTA CONFIDENTIAL

Quanta Computer Inc.			
PROJECT : CL1B			
Size	Document Number		Rev
	LCD CONNECTOR		3B
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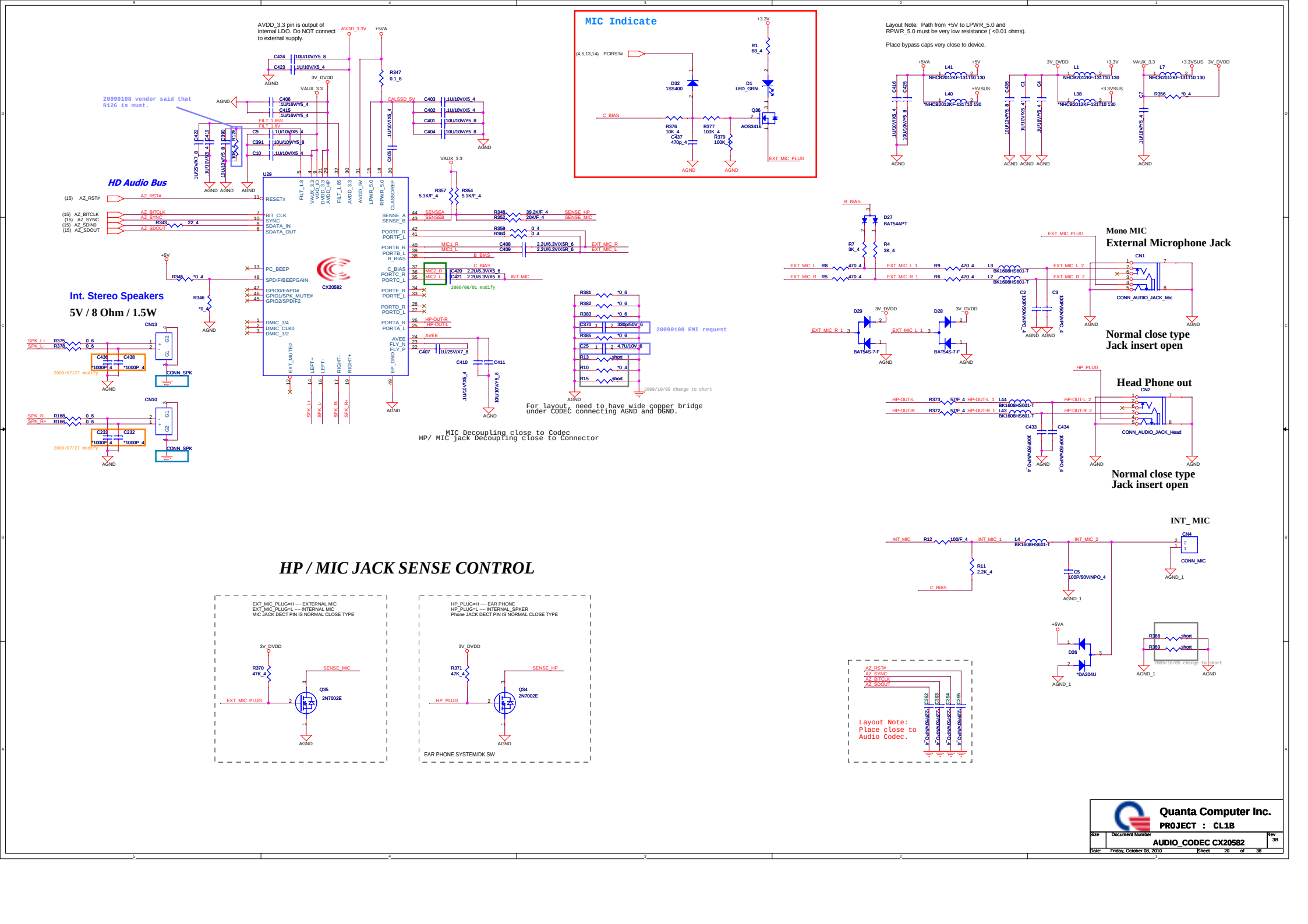
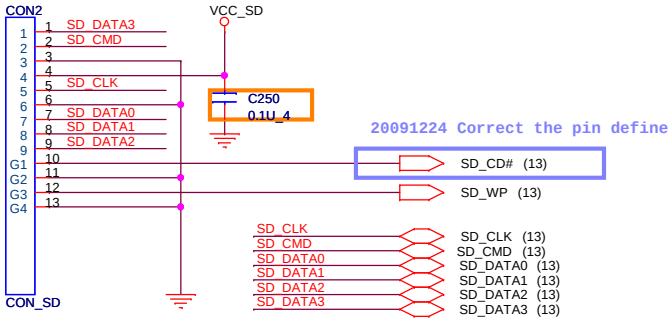
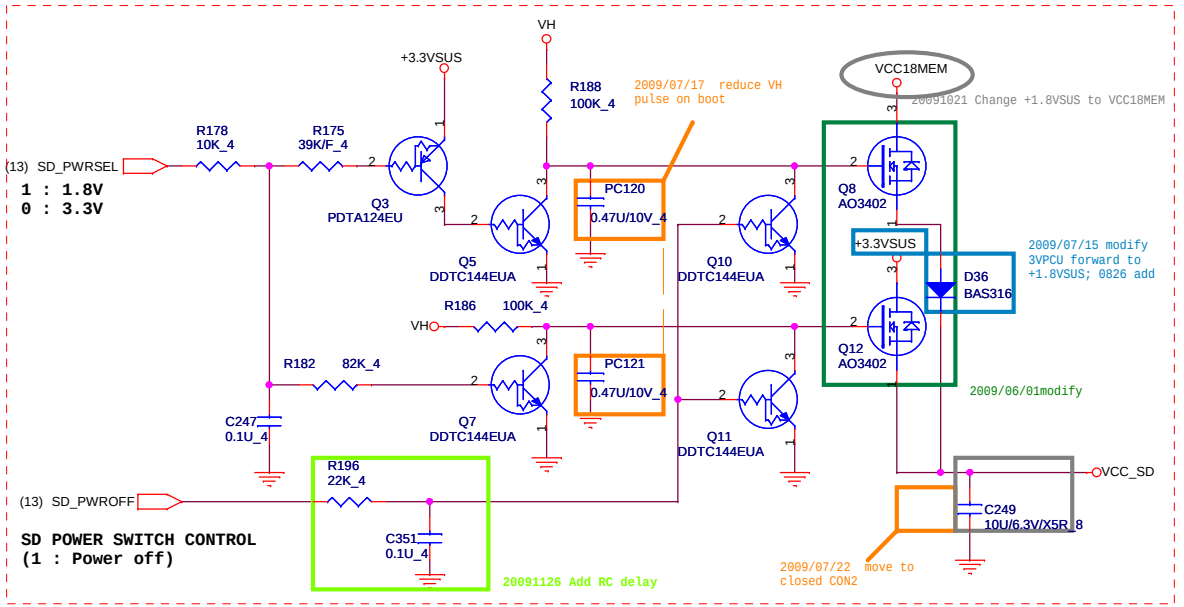
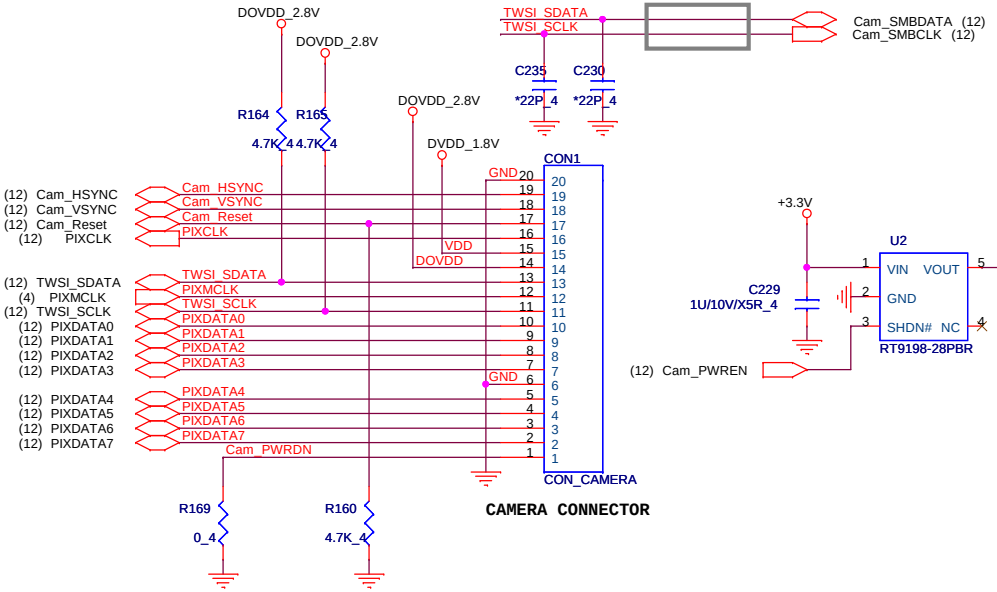

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.
20090108 vendor said that R126 is must.
HD Audio Bus
Int. Stereo Speakers
5V / 8 Ohm / 1.5W
CX20582
MIC Indicate
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).
Place bypass caps very close to device.
Mono MIC
External Microphone Jack
Normal close type
Jack insert open
Head Phone out
Normal close type
Jack insert open
INT_ MIC
HP / MIC JACK SENSE CONTROL
EXT_MIC_PLUG=H ---- EXTERNAL MIC
EXT_MIC_PLUG=L ---- INTERNAL MIC
MIC JACK DECT PIN IS NORMAL CLOSE TYPE
HP_PLUG=H ---- EAR PHONE
HP_PLUG=L ---- INTERNAL_SPKER
Phone JACK DECT PIN IS NORMAL CLOSE TYPE
EAR PHONE SYSTEM/DK SW
2009/06/01 modify
2009/10/05 change to short
20090108 EMI request
For layout , need to have wide copper bridge under CODEC connecting AGND and DGND.
MIC Decoupling close to Codec
HP/ MIC jack Decoupling close to Connector
Layout Note: Place close to Audio Codec.
Quanta Computer Inc.
PROJECT : CL1B
AUDIO_CODEC CX20582
Friday, October 08, 2010



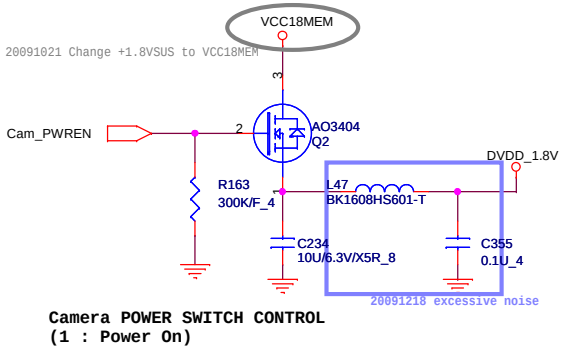
SD Write Protect Detection
(0 : Write Enable, 1 : Write Protect)



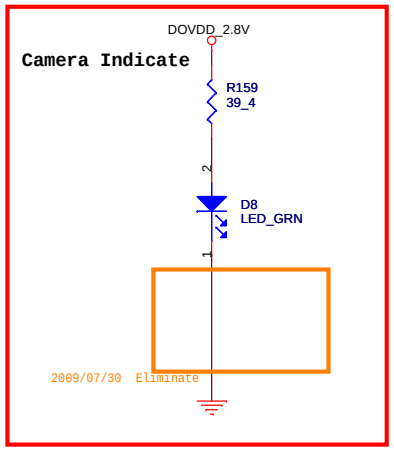
SD POWER SWITCH CONTROL
(1 : Power off)



CAMERA CONNECTOR



Camera POWER SWITCH CONTROL
(1 : Power On)



QUANTA CONFIDENTIAL

Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number	Rev
	NAND FLASH/SD/CAMERA	3B
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Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	NAND FLASH	3B

Date: Friday, October 08, 2010 Sheet 22 of 38

EC_ID

EC ID1	Setting
A	1/8*3VPCU
B1	2/8*3VPCU
B3	3/8*3VPCU
C1	4/8*3VPCU
C2	5/8*3VPCU
C2	6/8*3VPCU
C3	7/8*3VPCU

EC ID0	Setting
CL1A	
B2	1/2*3VPCU
B3	0
B4	1/8*3VPCU
C1	2/8*3VPCU
C2	3/8*3VPCU
CL1B	
B1	8/8*3VPCU

EC_RST#

08/05 depopulate due to ME issue

KEY PAD

KEY_RT_L, KEY_UP_L, KEY_DN_R, KEY_LF_L, KEY_RT_R, KEY_UP_R, KEY_DN_L, KEY_LF_R, KEY_ROTATE, POWER_BUTTON#

MR Sensor

S1 MRSS20Z, S2 MRSS20Z

EEPROM 24C01

2009/09/23 Correct part reference and footprint

20090610 Change P/N

Spansion SPI

U23 S25FL008A0LMFI003

EC UART Debug port

3700 : PIN 23 : TXD

LED

KEYBOARD AND TOUCH PAD

KB3700 64-pin LQFP

USB to SPI writer Connector to update EC F/W

R591
POP : Normal
DEPOP : Update EC F/W

*NA/HEADER 4X2 (Pitch 2.54mm)

EMI RESERVED

Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	EC_KB3700	3B

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GPIO[2] boot-up configuration:
0: JTAG mode enabled (pulled low by 100kohms)
1 and floating: JTAG mode disabled (Default)

[ANT_SEL_N, TR3n] boot-up configuration:
00: General SPI (pulled-low by 100kohms)
11: SDIO (floating is ok)

GPIO[4]:
WLAN MAC wake-up input/interrupt input

ECSn boot-up configuration:
0: Boot up from SPI EEPROM (pulled-low by 100kohms)
1 & floating: Boot up from host interface (Default)

ANT_SEL_N R326 *100K_4
TR3n R324 *100K_4
ECSn R323 *100K_4
WL_GPIO2 R338 *100K_4

Only for SDIO & USB device

20091015 Correct all WLAN schematic

CN19

T90	1	GPIO[4]	2 +3.3V
T91	3	BT_PRIORITY	4 GND
T92	5	WL_ACTIVE	6 1.8V/NC
T93	7	BT_STATE	8 TRSTn
	9	GND	10 TMS_CPU
	11	NC	12 TCK
	13	NC	14 TDO
	15	GND	16 TDI
(13) SDDA_CD#	17	SD_CD (SD Card Detection)	18 GND
	19	GND	20 PDn
(13) SDDA_CLK	21	SD_CLK/SPI_CLK	22 RESETn
	23	GND	24 3.3V
(13) SDDA_CMD	25	SD_CMD/SPI_SDI	26 GND
(13) SDDA_D0	27	SD_DAT[0]/SPI_SCSn	28 1.8V/NC
(13) SDDA_D1	29	SD_DAT[1]/SPI_SDO	30 NC
(13) SDDA_D2	31	SD_DAT[2]/SPI_SINTn	32 NC
(13) SDDA_D3	33	SD_DAT[3]	34 GND
	35	GND	36 USB_D-
	37	GND	38 USB_D+
	39	3.3V	40 GND
	41	3.3V	42 NC
	43	GND	44 GPIO[1] (LED_WLAN#)
T89 WL_GPIO2	45	GPIO[2]	46 NC
T94 ECSn	47	ECSn	48 SLEEP_CLK
T96 TR3n	49	TR3n	50 GND
T97 ANT_SEL_N	51	ANT_SEL_N	52 3.3V

KEY

IC SOCKET MINI PCIE EXP 52P(P0.8,H5.0)
20-25096-00

WLAN_3.3V place at CN19.2
C455 0.1U/10V_4
VA18
C456 0.1U/10V_4
TRSTn T17
TMS_CPU T47
TCK T48
TDO T80
TDI T82
PR156 *100K_4
PR48 10K_4
20091125 Prevent the leakage of WLAN_3.3V
D41 1SS400
PDn
WLAN_RESET# (15)
C454 0.1U/10V_4 place at CN19.24
C458 0.1U/10V_4 place at CN19.28
WL_USBP5- (15)
WL_USBP5+ (15)
LED_WLAN#
T95
C238 0.1U/10V_4 place at CN19.52
C385 0.1U/10V_4 place at CN19.39
WLAN_3.3V

VCC18MEM
20091021 Change +1.8VSUS to VCC18MEM
Q37 AO3420
L45 NHCB2012KF-131T10 130
VA18
C453 10U/6.3V/X5_8
R389 47K_4
C368 *0.1U
WLAN_3.3V
20091230 for WLAN power sequence

+3.3VSUS
VH
R388 100K_4
20091231 chnge to 0.47ufK to prevent the giltch of WLAN_3.3V
WLAN_PW
AO3404 Q29
1: power off
0: power on
(13) WLAN_EN
R380 47K_4
Q38 CHDTC144EUPT
C331 0.1U
20091125 for WLAN glitch when resuming
C446 0.47U/10V_4
C452 10U/6.3V/X5_8
C457 *2200P
20091218 delete R387 due to no enough spaceng
WLAN_3.3V

VIN
D2 LED_GREEN
D3 LED_GREEN
LED 10
LED 13
D24 LED_GREEN
WLAN LED
D23 LED_GREEN
HDD LED
LED 11
LED 14
R365 510_4
R344 510_4
LED 12
LED 15
20091229 To prevent the leakage of WLAN_3.3V, change +3.3V to WLAN_3.3V
WLAN_3.3V
+3.3V
LED_WLAN#
D38 1SS400
Q40 PDTA124EU
(13,14) HDD_LED#/GPIO11
Q32 PDTA124EU
Q33 DDTC144EUA
Q30 DDTC144EUA

Future Hacking

+5VSUS
R392 *0_8
R393 *0_8
HA_USBP4+ (15)
HA_USBP4- (15)
20090730 Add

MICRO_SD_3.3V
CON3
(13) MSD_D2
(13) MSD_D3
(13) MSD_CMD
(13) MSD_CLK
(13) MSD_D0
(13) MSD_D1
DAT2
CD/ DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
C379 0.1U_4
CONN MICRO-SD 8P 1R FR(P1.1,H1.97)
20091009 modify and place at CON3.4.

+3.3VSUS
VH
R395 100K_4
0: power on
1: power off
(15,23) MSD_PWROFF
Q28 CHDTC144EUPT
AO3404 Q27
PC122 0.1U/10V_4
MICRO_SD_3.3V
C399 10U/6.3V/X5R_8
20091009 modify and place at CON3.4.

20100929 add a discarge circuit
MICRO_SD_3.3V
PR169 22_8
(15,23) MSD_PWROFF
PQ60 2N7002W

Quanta Computer Inc.
PROJECT : CL1B

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	WLAN 88W8388	3B
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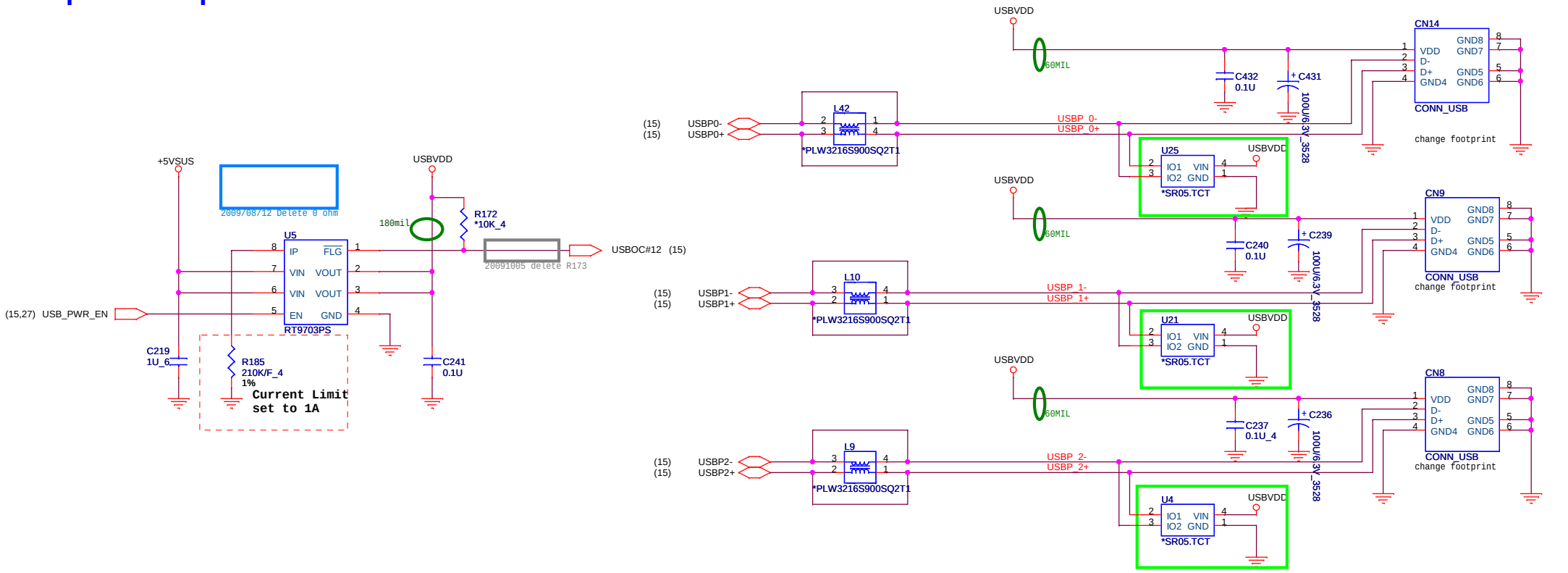
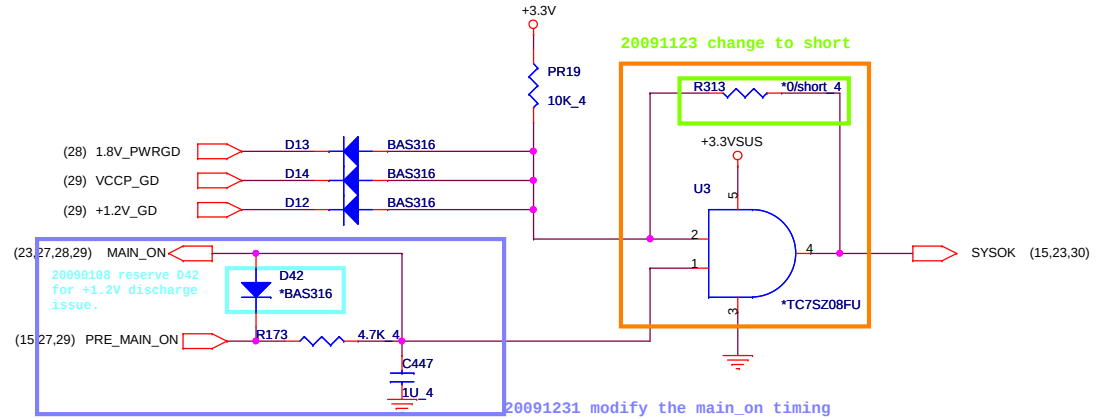
USB power / port



Reset circuit



Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	USB	3B
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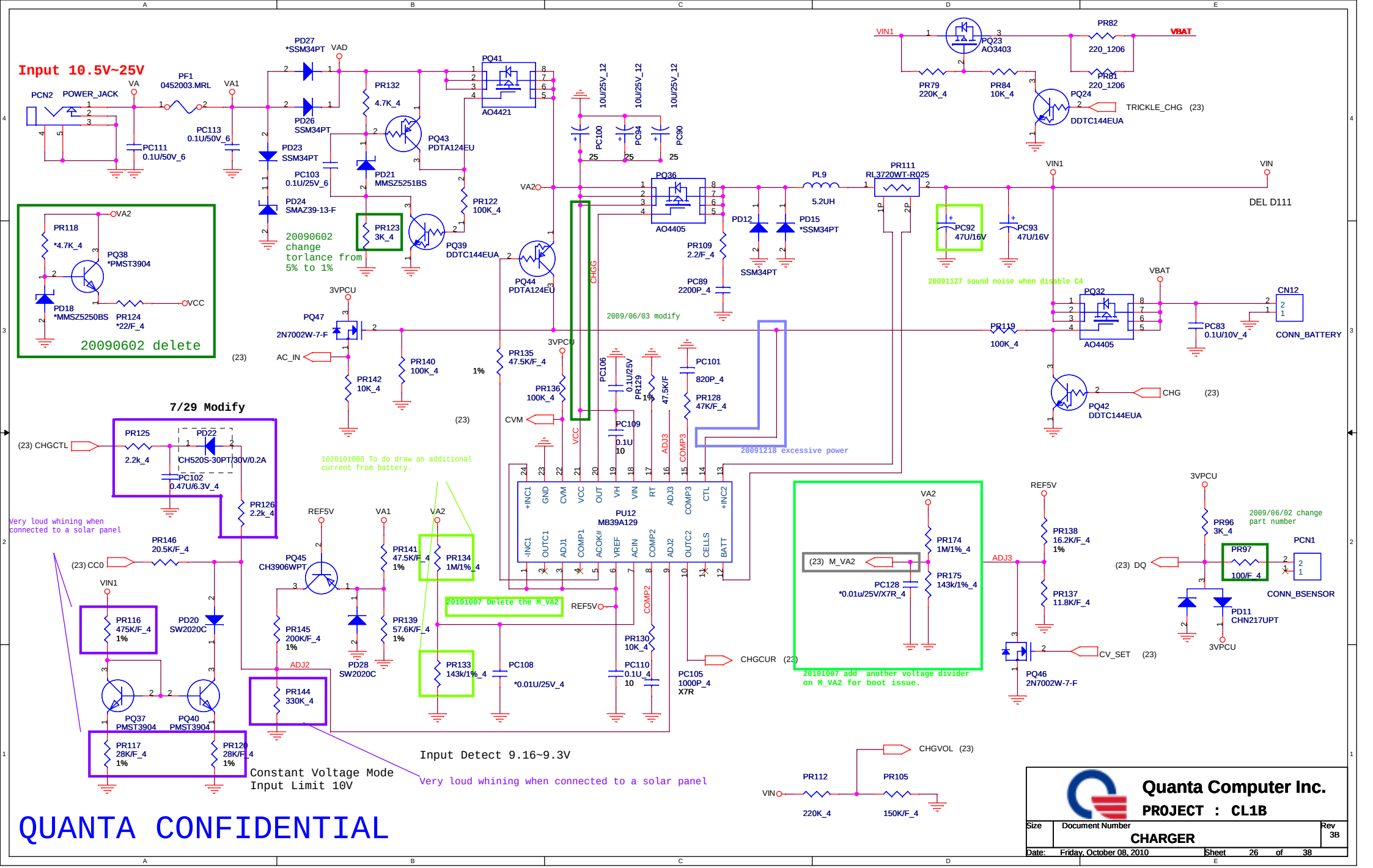
Input 10.5V~25V
PCN2 POWER_JACK
PF1 0452003.MRL
PC111 0.1U/50V_6
PC113 0.1U/50V_6
PD27 *SSM34PT
PD26 SSM34PT
PD23 SSM34PT
PD24 SMAZ39-13-F
PD21 MMSZ5251BS
PR132 4.7K_4
PQ43 PDTA124EU
PQ41 AO4421
PR122 100K_4
PR123 3K_4
PQ39 DDTC144EUA
20090602 change torlance from 5% to 1%
PR118 *4.7K_4
PQ38 *PMST3904
PD18 *MMSZ5250BS
PR124 *22/F_4
20090602 delete
PC100 10U/25V_12
PC94 10U/25V_12
PC90 10U/25V_12
PQ44 PDTA124EU
PQ36 AO4405
PD12
PD15 *SSM34PT
PR109 2.2/F_4
PC89 2200P_4
SSM34PT
PL9 5.2UH
PR111 RL3720WT-R025
PC92 47U/16V
PC93 47U/16V
20091127 sound noise when disable C4
PQ32 AO4405
PC83 0.1U/10V_4
CN12
CONN_BATTERY
PR119 100K_4
PQ42 DDTC144EUA
CHG (23)
PQ23 AO3403
PR79 220K_4
PR84 10K_4
PR82 220_1206
PR81 220_1206
PQ24 DDTC144EUA
TRICKLE_CHG (23)
DEL D111
2009/06/03 modify
PQ47 2N7002W-7-F
AC_IN (23)
PR140 100K_4
PR142 10K_4
PR135 47.5K/F_4
PR136 100K_4
PC106 0.1U/25V
PR129 47.5K/F_4
PC101 820P_4
PR128 47K/F_4
PC109 0.1U 10
20091218 excessive power
1020101008 To do draw an additional current from battery.
7/29 Modify
PR125 2.2k_4
PD22 CH520S-30PT/30V/0.2A
PC102 0.47U/6.3V_4
PR126 2.2k_4
(23) CHGCTL
Very loud whining when connected to a solar panel
PR146 20.5K/F_4
(23) CC0
PR116 475K/F_4 1%
PD20 SW2020C
PR117 28K/F_4 1%
PR120 28K/F_4 1%
PQ37 PMST3904
PQ40 PMST3904
PR144 330K_4
ADJ2
PQ45 CH3906WPT
PR145 200K/F_4 1%
PD28 SW2020C
PR141 47.5K/F_4 1%
PR139 57.6K/F_4 1%
PR134 1M/1%_4
PR133 143k/1%_4
PC108 *0.01U/25V_4
20101007 Delete the M_VA2
PU12 MB39A129
+INC1 GND CVM VCC OUT VH VIN RT ADJ3 COMP3 CTL +INC2
+INC1 OUTC1 ADJ1 COMP1 ACOK# VREF ACIN COMP2 ADJ2 OUTC2 CELLS BATT
PR130 10K_4
PC110 0.1U_4 10
PC105 1000P_4 X7R
CHGCUR (23)
(23) M_VA2
PR174 1M/1%_4
PR175 143k/1%_4
PC128 *0.01u/25V/X7R_4
20101007 add another voltage divider on M_VA2 for boot issue.
PR138 16.2K/F_4 1%
PR137 11.8K/F_4
PQ46 2N7002W-7-F
CV_SET (23)
PR96 3K_4
2009/06/02 change part number
PR97 100/F_4
PCN1
(23) DQ
CONN_BSENSOR
PD11 CHN217UPT
CHGVOL (23)
PR112 220K_4
PR105 150K/F_4
Input Detect 9.16~9.3V
Very loud whining when connected to a solar panel
Constant Voltage Mode
Input Limit 10V
QUANTA CONFIDENTIAL
Quanta Computer Inc.
PROJECT : CL1B
Size
Document Number
CHARGER
Rev 3B
Date: Friday, October 08, 2010
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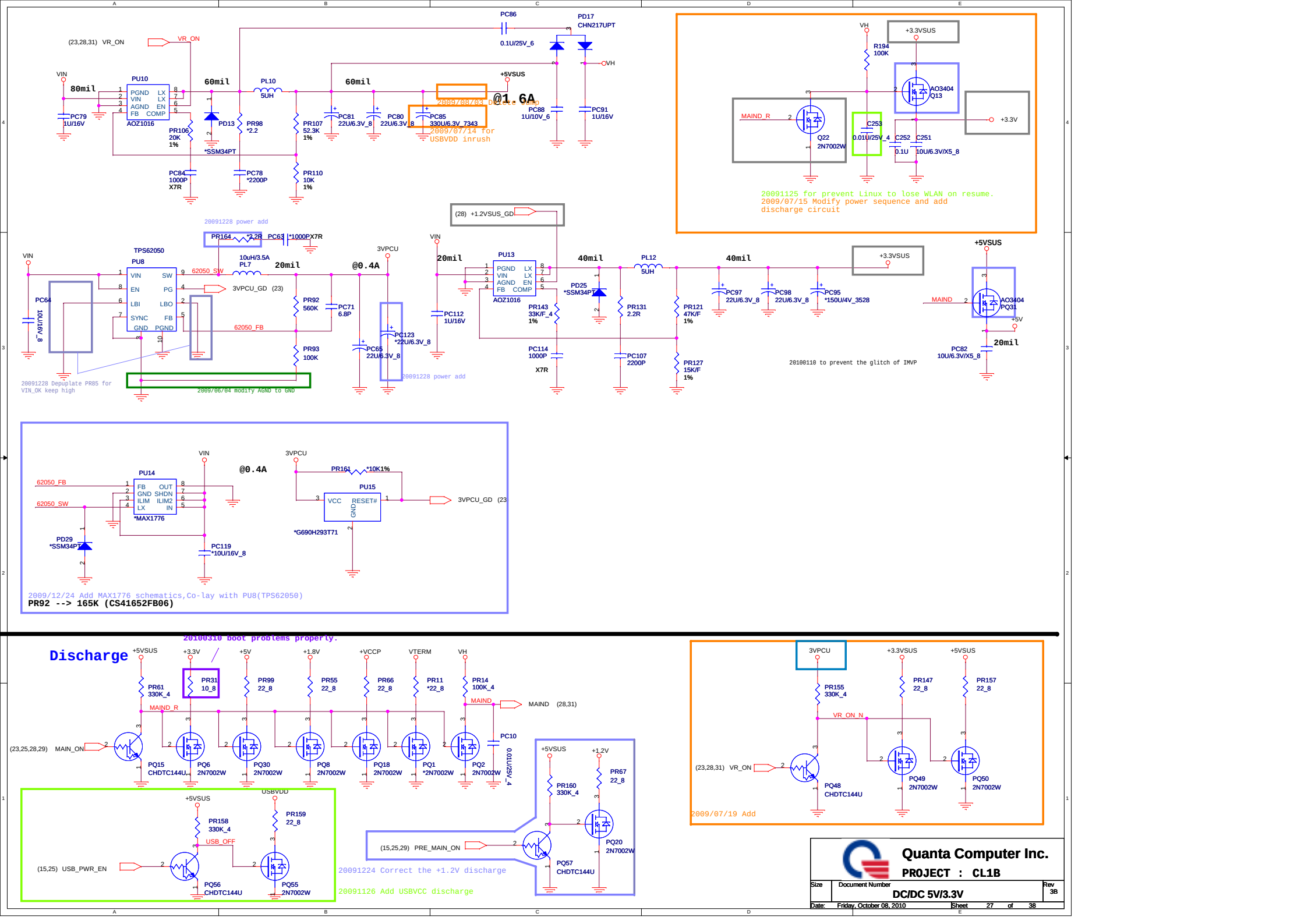
(23,28,31) VR_ON
VR_ON
VIN
80mil
PU10
PGND LX
VIN LX
AGND EN
FB COMP
AOZ1016
PC79
1U/16V
PR106
20K
1%
PD13
*SSM34PT
60mil
PL10
5UH
PR98
*2.2
PR107
52.3K
1%
PC84
1000P
X7R
PC78
*2200P
PR110
10K
1%
60mil
PC81
22U/6.3V_8
PC80
22U/6.3V_8
PC85
330U/6.3V_7343
2009/07/14 for
USBVDD inrush
PC86
0.1U/25V_6
PD17
CHN217UPT
VH
+5VSUS
@1.6A
PC88
1U/10V_6
PC91
1U/16V
20091228 power add
PR164
*2.2R
PC63
*1000PX7R
TPS62050
PU8
VIN SW
EN PG
LBI LBO
SYNC FB
GND PGND
10uH/3.5A
PL7
20mil
@0.4A
3VPCU
62050_SW
3VPCU_GD (23)
62050_FB
PR92
560K
PC71
6.8P
PR93
100K
PC64
10U/16V_8
PC65
22U/6.3V_8
PC123
*22U/6.3V_8
20091228 Depuplate PR85 for
VIN_OK keep high
2009/06/04 modify AGND to GND
20091228 power add
(28) +1.2VSUS_GD
VIN
20mil
PU13
PGND LX
VIN LX
AGND EN
FB COMP
AOZ1016
PC112
1U/16V
40mil
PL12
5UH
40mil
PD25
*SSM34PT
PR143
33K/F_4
1%
PC114
1000P
X7R
PR131
2.2R
PC107
2200P
PR121
47K/F
1%
PR127
15K/F
1%
PC97
22U/6.3V_8
PC98
22U/6.3V_8
PC95
*150U/4V_3528
20100110 to prevent the glitch of IMVP
+3.3VSUS
+5VSUS
MAIND
AO3404
PQ31
+5V
20mil
PC82
10U/6.3V/X5_8
VH
+3.3VSUS
R194
100K
AO3404
Q13
MAIND_R
Q22
2N7002W
C253
0.01U/25V_4
C252
0.1U
C251
10U/6.3V/X5_8
+3.3V
20091125 for prevent Linux to lose WLAN on resume.
2009/07/15 Modify power sequence and add
discharge circuit
VIN
@0.4A
PU14
FB OUT
GND SHDN
ILIM ILIM2
LX IN
*MAX1776
62050_FB
62050_SW
PD29
*SSM34PT
PC119
*10U/16V_8
3VPCU
PR161
*10K1%
PU15
VCC RESET#
GND
3VPCU_GD (23
*G690H293T71
2009/12/24 Add MAX1776 schematics,Co-lay with PU8(TPS62050)
PR92 --> 165K (CS41652FB06)
20100310 boot problems properly.
Discharge
+5VSUS
+3.3V
+5V
+1.8V
+VCCP
VTERM
VH
PR61
330K_4
PR31
10_8
PR99
22_8
PR55
22_8
PR66
22_8
PR11
*22_8
PR14
100K_4
MAIND_R
MAIND
MAIND (28,31)
PC10
0.01U/25V_4
(23,25,28,29) MAIN_ON
PQ15
CHDTC144U
PQ6
2N7002W
PQ30
2N7002W
PQ8
2N7002W
PQ18
2N7002W
PQ1
*2N7002W
PQ2
2N7002W
USBVDD
PR158
330K_4
PR159
22_8
USB_OFF
(15,25) USB_PWR_EN
PQ56
CHDTC144U
PQ55
2N7002W
+5VSUS
+1.2V
PR160
330K_4
PR67
22_8
(15,25,29) PRE_MAIN_ON
PQ57
CHDTC144U
PQ20
2N7002W
20091224 Correct the +1.2V discharge
20091126 Add USBVCC discharge
3VPCU
+3.3VSUS
+5VSUS
PR155
330K_4
PR147
22_8
PR157
22_8
VR_ON_N
(23,28,31) VR_ON
PQ48
CHDTC144U
PQ49
2N7002W
PQ50
2N7002W
2009/07/19 Add
Quanta Computer Inc.
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DC/DC 5V/3.3V
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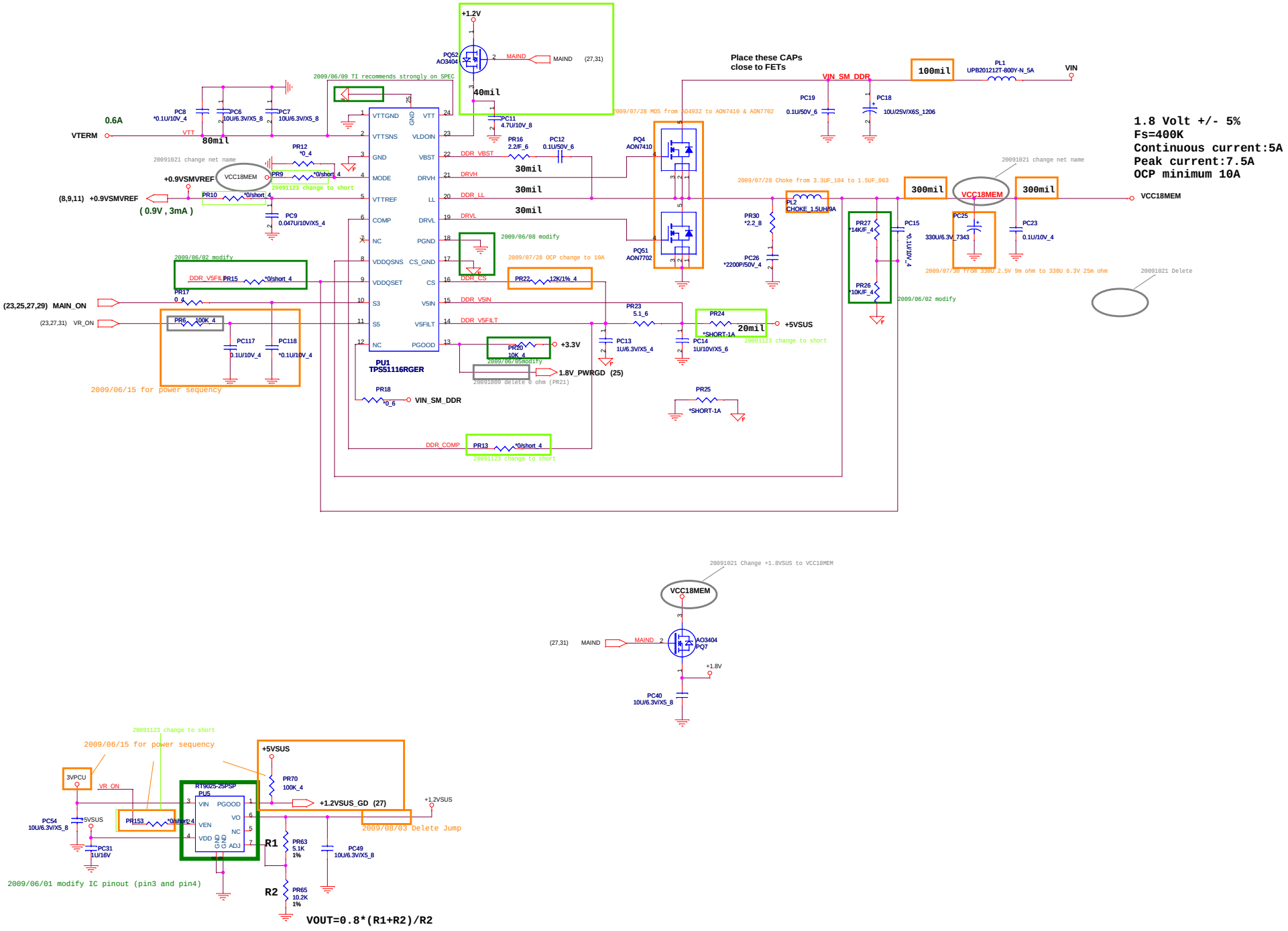

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	DDRII/+0.9V(TPS51116)	3B
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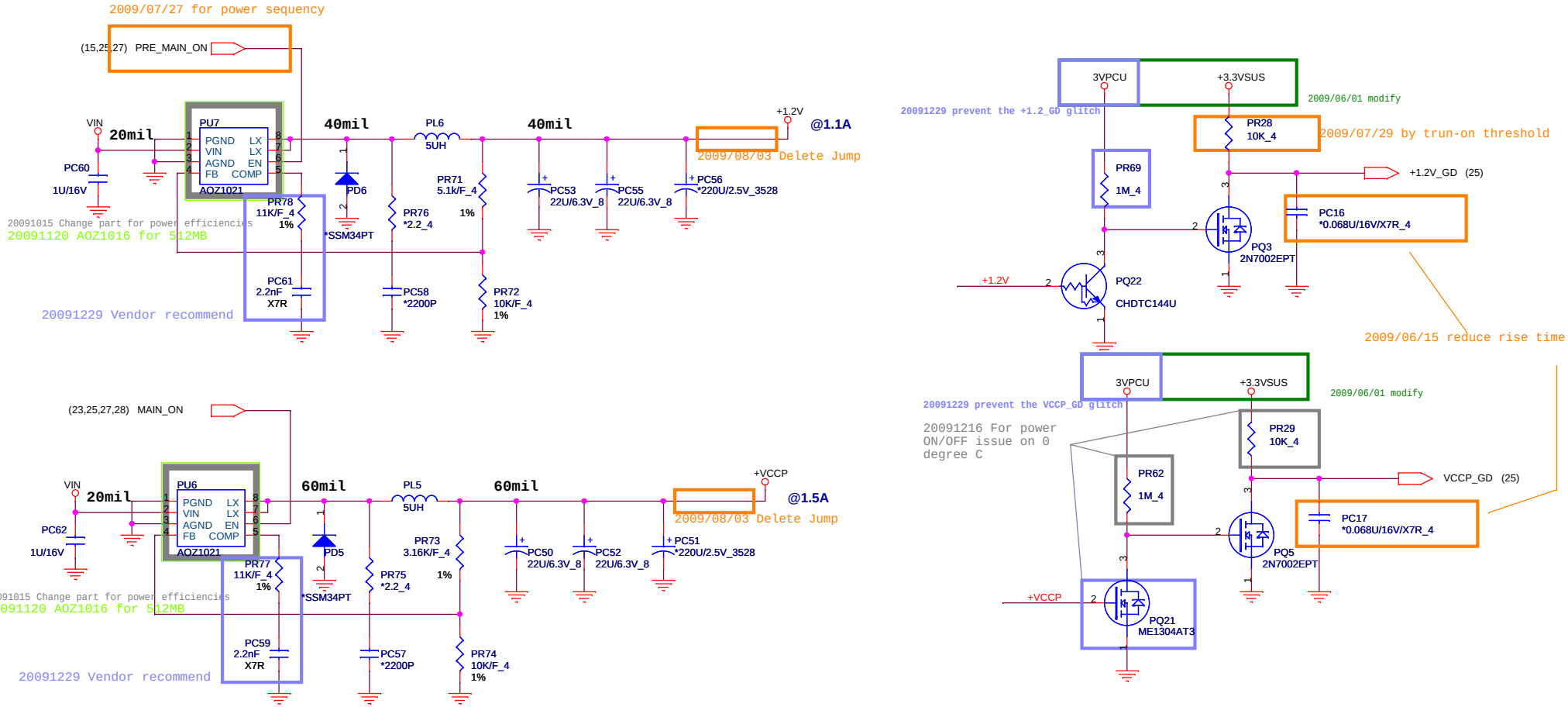

Vo=0.8 x (1+(R2/R3))

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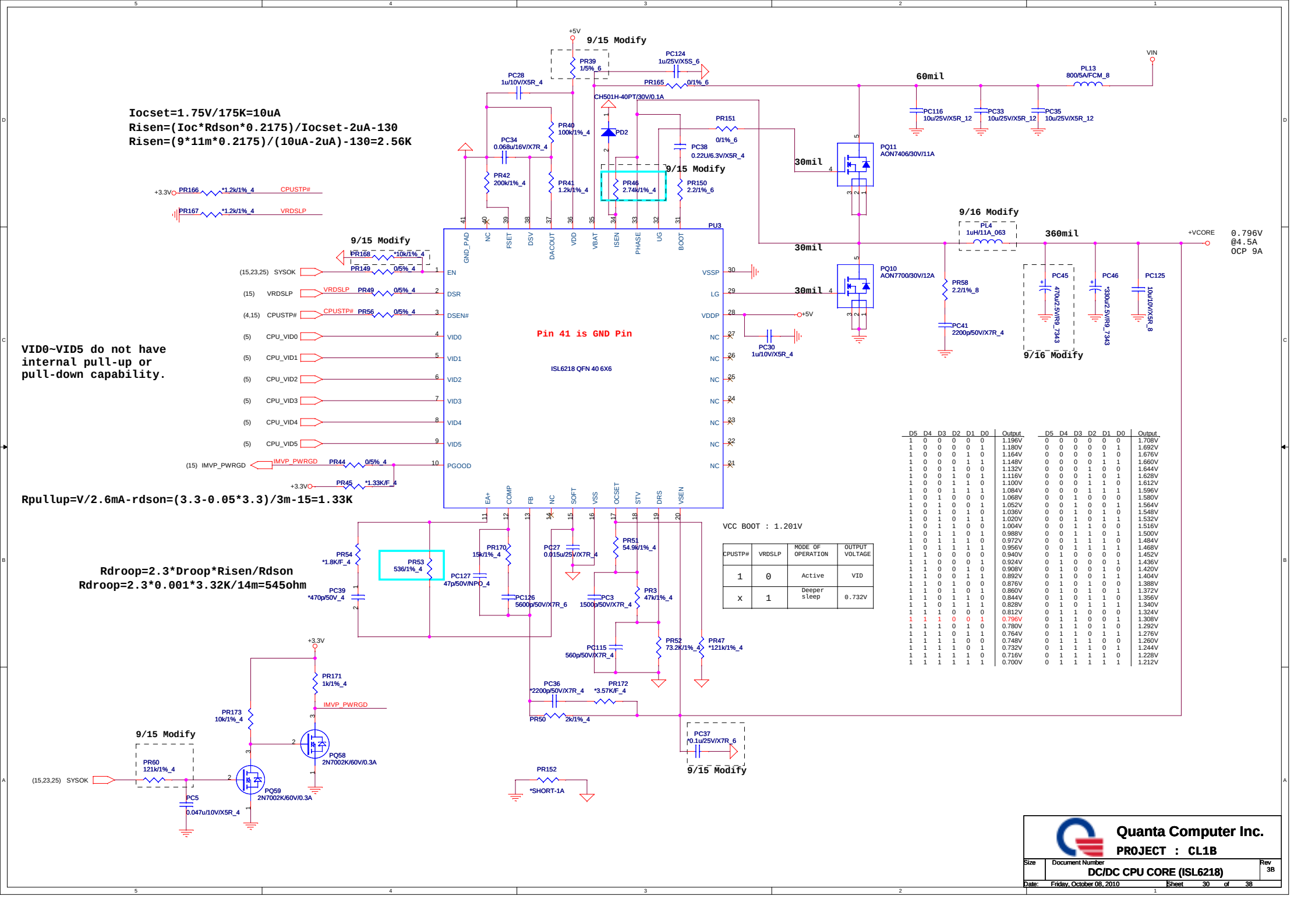
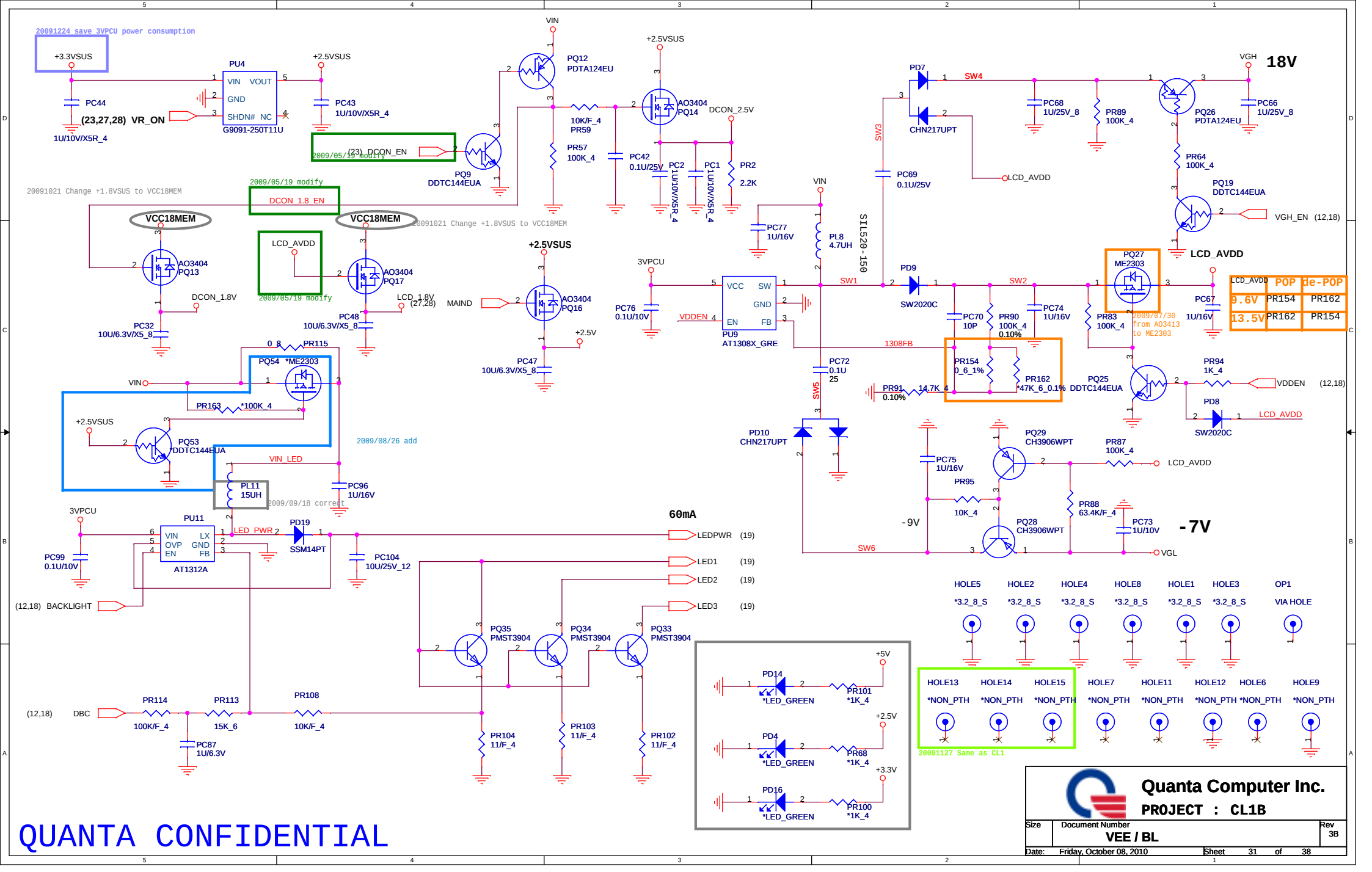


CPUSTP#	VRDSLP	MODE OF OPERATION	OUTPUT VOLTAGE
1	0	Active	VID
x	1	Deeper sleep	0.732V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V
1	0	0	0	0	1	1.180V
1	0	0	0	1	0	1.164V
1	0	0	0	1	1	1.148V
1	0	0	1	0	0	1.132V
1	0	0	1	0	1	1.116V
1	0	0	1	1	0	1.100V
1	0	0	1	1	1	1.084V
1	0	1	0	0	0	1.068V
1	0	1	0	0	1	1.052V
1	0	1	0	1	0	1.036V
1	0	1	0	1	1	1.020V
1	0	1	1	0	0	1.004V
1	0	1	1	0	1	0.988V
1	0	1	1	1	0	0.972V
1	0	1	1	1	1	0.956V
1	1	0	0	0	0	0.940V
1	1	0	0	0	1	0.924V
1	1	0	0	1	0	0.908V
1	1	0	0	1	1	0.892V
1	1	0	1	0	0	0.876V
1	1	0	1	0	1	0.860V
1	1	0	1	1	0	0.844V
1	1	0	1	1	1	0.828V
1	1	1	0	0	0	0.812V
1	1	1	0	0	1	0.796V
1	1	1	0	1	0	0.780V
1	1	1	0	1	1	0.764V
1	1	1	1	0	0	0.748V
1	1	1	1	0	1	0.732V
1	1	1	1	1	0	0.716V
1	1	1	1	1	1	0.700V

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.708V
0	0	0	0	0	1	1.692V
0	0	0	0	1	0	1.676V
0	0	0	0	1	1	1.660V
0	0	0	1	0	0	1.644V
0	0	0	1	0	1	1.628V
0	0	0	1	1	0	1.612V
0	0	0	1	1	1	1.596V
0	0	1	0	0	0	1.580V
0	0	1	0	0	1	1.564V
0	0	1	0	1	0	1.548V
0	0	1	0	1	1	1.532V
0	0	1	1	0	0	1.516V
0	0	1	1	0	1	1.500V
0	0	1	1	1	0	1.484V
0	0	1	1	1	1	1.468V
0	1	0	0	0	0	1.452V
0	1	0	0	0	1	1.436V
0	1	0	0	1	0	1.420V
0	1	0	0	1	1	1.404V
0	1	0	1	0	0	1.388V
0	1	0	1	0	1	1.372V
0	1	0	1	1	0	1.356V
0	1	0	1	1	1	1.340V
0	1	1	0	0	0	1.324V
0	1	1	0	0	1	1.308V
0	1	1	0	1	0	1.292V
0	1	1	0	1	1	1.276V
0	1	1	1	0	0	1.260V
0	1	1	1	0	1	1.244V
0	1	1	1	1	0	1.228V
0	1	1	1	1	1	1.212V


20091224 save 3VPCU power consumption
+3.3VSUS
PU4
VIN VOUT
GND
SHDN# NC
G9091-250T11U
+2.5VSUS
PC44
1U/10V/X5R_4
(23,27,28) VR_ON
PC43
1U/10V/X5R_4
(23) DCON_EN
2009/05/19 modify
PQ9
DDTC144EUA
VIN
PQ12
PDTA124EU
10K/F_4
PR59
PR57
100K_4
AO3404
PQ14
DCON_2.5V
PC42
0.1U/25V
PC2
1U/10V/X5R_4
PC1
1U/10V/X5R_4
PR2
2.2K
20091021 Change +1.8VSUS to VCC18MEM
2009/05/19 modify
DCON_1.8_EN
VCC18MEM
AO3404
PQ13
DCON_1.8V
PC32
10U/6.3V/X5_8
LCD_AVDD
2009/05/19 modify
AO3404
PQ17
LCD_1.8V
(27,28) MAIND
PC48
10U/6.3V/X5_8
20091021 Change +1.8VSUS to VCC18MEM
+2.5VSUS
AO3404
PQ16
+2.5V
PC47
10U/6.3V/X5_8
0_8
PR115
PQ54 *ME2303
VIN
PR163
*100K_4
+2.5VSUS
PQ53
*DDTC144EUA
2009/08/26 add
VIN_LED
PL11
15UH
2009/09/18 correct
PC96
1U/16V
3VPCU
PU11
VIN LX
OVP GND
EN FB
AT1312A
LED_PWR
PD19
SSM14PT
PC99
0.1U/10V
PC104
10U/25V_12
60mA
LEDPWR (19)
LED1 (19)
LED2 (19)
LED3 (19)
(12,18) BACKLIGHT
PQ35
PMST3904
PQ34
PMST3904
PQ33
PMST3904
(12,18) DBC
PR114
100K/F_4
PR113
15K_6
PR108
10K/F_4
PC87
1U/6.3V
PR104
11/F_4
PR103
11/F_4
PR102
11/F_4
PD14
*LED_GREEN
PR101
*1K_4
+5V
PD4
*LED_GREEN
PR68
*1K_4
+2.5V
PD16
*LED_GREEN
PR100
*1K_4
+3.3V
VIN
PC77
1U/16V
PL8
4.7UH
SI1520-150
3VPCU
PC76
0.1U/10V
VDDEN
PU9
AT1308X_GRE
VCC SW
GND
EN FB
SW1
1308FB
PC72
0.1U
25
SW5
PD10
CHN217UPT
PD7
SW4
CHN217UPT
SW3
PC69
0.1U/25V
LCD_AVDD
PC68
1U/25V_8
PR89
100K_4
PQ26
PDTA124EU
VGH
18V
PC66
1U/25V_8
PR64
100K_4
PQ19
DDTC144EUA
VGH_EN (12,18)
LCD_AVDD
PD9
SW2020C
SW2
PQ27
ME2303
PC70
10P
PR90
100K_4
0.10%
PC74
1U/16V
PR83
100K_4
2009/07/30
from AO3413
to ME2303
PC67
1U/16V
LCD_AVDD
POP
de-POP
9.6V
PR154
PR162
13.5V
PR162
PR154
PR91
14.7K_4
0.10%
PR154
0_6_1%
PR162
*47K_6_0.1%
PQ25
DDTC144EUA
PR94
1K_4
VDDEN (12,18)
PD8
SW2020C
LCD_AVDD
PQ29
CH3906WPT
PR87
100K_4
LCD_AVDD
PC75
1U/16V
PR95
10K_4
-9V
PQ28
CH3906WPT
PR88
63.4K/F_4
PC73
1U/10V
-7V
SW6
VGL
HOLE5
*3.2_8_S
HOLE2
*3.2_8_S
HOLE4
*3.2_8_S
HOLE8
*3.2_8_S
HOLE1
*3.2_8_S
HOLE3
*3.2_8_S
OP1
VIA HOLE
HOLE13
*NON_PTH
HOLE14
*NON_PTH
HOLE15
*NON_PTH
HOLE7
*NON_PTH
HOLE11
*NON_PTH
HOLE12
*NON_PTH
HOLE6
*NON_PTH
HOLE9
*NON_PTH
20091127 Same as CL1
QUANTA CONFIDENTIAL
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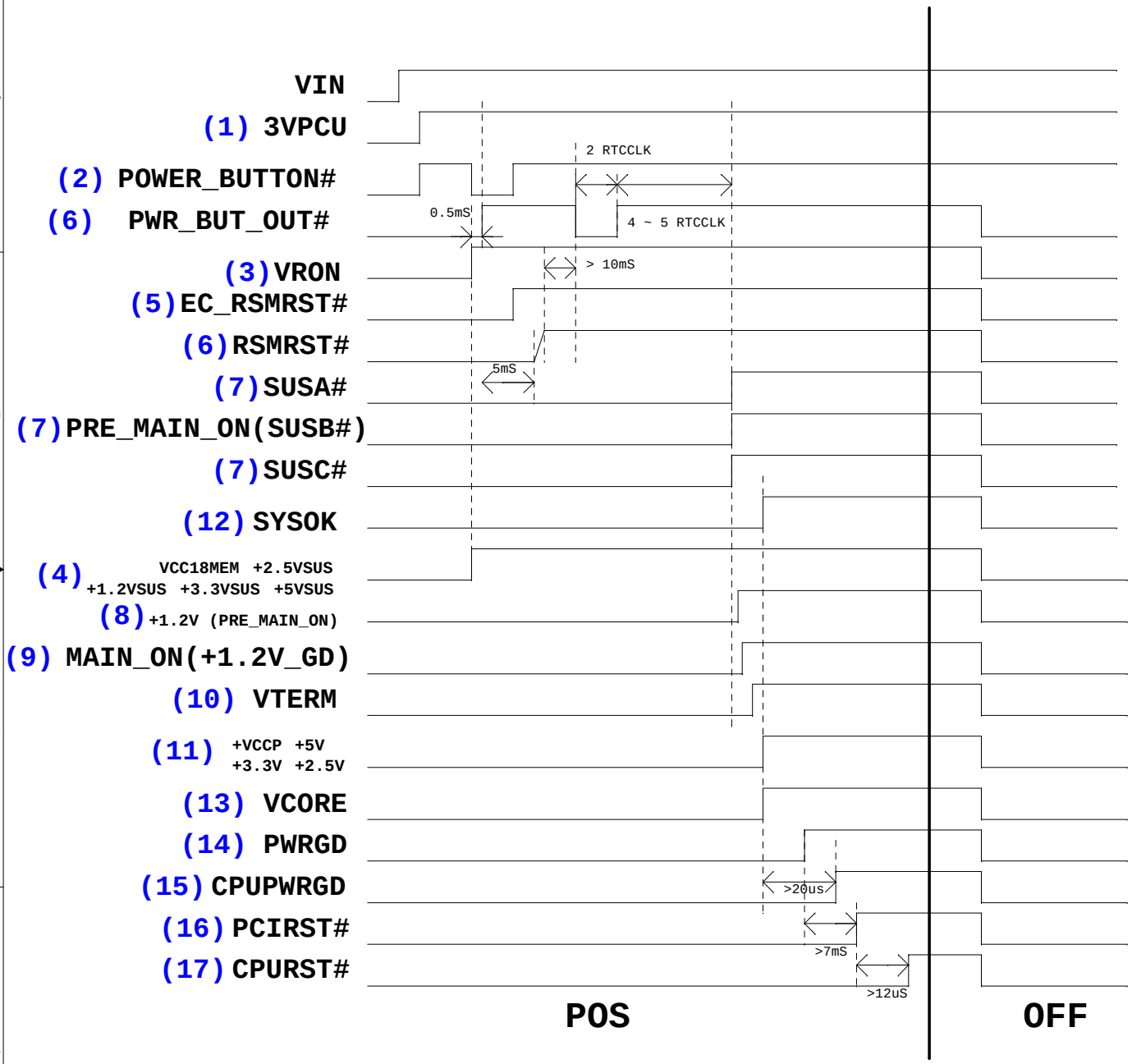

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Schematic modify Item and History :

A1-->A2

1. *DCON POWER -*
   - A. Change PQ9.B pin from DCON_1.8 to DCON_EN
   - B. Change PQ13.G pin from DCON_EN to PQ12.C
   - C. Change PQ17.G pin from VDDEN to LCD_AVDD
2. *SB straping -*
   - A. Change R27, R83, R270, R54, R34, R87, R78 and R82 from 4.7K ohm to 1K ohm.
3. *Design issue -*
   - A.The D pin and S pin of Q8 and Q12 is inverse
   - B.Change C299 part number
   - C.Add test points: U28, pins 1, 4, 17, 29, 36, and 37
   - d.Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L
   - e.RTC issue: VIA recommend to delete R216
4. *Power -*
   - A.1.8VSUS
     - a. Add off-page connector : VR_ON
     - b. Modify PU5 pinout.
     - C. For +1.8VUSU sense: stuff PR15 ; don't stuff PR27 and PR26
     - d. For +1.8VUSU OCP : modify PR22 from 4.99K to 6.2K, OCP from 3A to 3.5A
     - e. modify PU1 pin11 net name to VR_ON
   - B.+VCORE:
     - a.For SYSOK PULL HIGH: Stuff PR45
     - b.For +VCORE sense: don't stuff PC3 & PR3 ; stuff PR51 & PR52
     - c.For CPU Load line : for meet load line -1mV/A, modify PR52 & PR50 from 1K to 680 ohm
   - C.1.2 and +VCCP:
     - a.Modify power good circuit: change net name from 3.3VSUS to +3.3VSUS
   - D.Charger :
     - a.Delete clamp circuit (PR118,PD18,PQ38,PR124):
       PU12 (MB39A129) can guaranty to 28V
     - b.connect PU12 pin21 to PQ36 pin1,2,3 directly
     - c.change PR126 to 100K
5. *WLAN-*
   - Change WLAN solution from SD card to TM100 module. See page 24

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Schematic modify Item and History :

A2-->B1

2. SDIO

A. SDIO:Micro SD
B. SDIO1: SD Card Reader
C. SDIO2: WLAN module

2. SB straping -

A. Change R58, R170 and R195 pull up power plane on page13

3. Design issue -

A.Modify CPU RST circuit
  a.Add R248 0 ohm
  b.Populate Q18,Q20 R275 to prevent leakage for vendor's recommand.
  c.Del c299 for CPU power good delay time
B.Del SPI ROM of memory
C.Modify DCONLOAD and WLAN_RESET# to U19.AG20 and AF21
D.Modify Serial enable to U19.AJ21
E.Modify THRM# pin of U19 from PROCHOT# to EB_MODE
F.Del EDID_CLK and EDID_DATA of CRT circuit
G.Del R195 within GDATA0 pull low
H.Rerevse C436,C438, C233 and C232 for EMI/ESD
I.Add PC120 and PC121 for VH gilch and add D36 to prevent 3VPU forward to +1.8VSUS
J.Move C250 to close CON2 and modify CAM LED control.
K.Del NAND flash on page 22
L.Add PWRGD net on U28.17 & SYSOK on U28.4 & change M/B ID & Del SW7 on page 23
M. change Q14 from PNP BJT to P-MOS
N. Change WLAN solution from on board to slot and correct WLAN LED behavior on page 24.
O. Add Micro SD on page 24.
P. Correct power good circuit on page 25.

4. Power -

A.Del all jump,but only reserve the jump of +VCCORE and +1.8VSUS.

A.1.8VSUS
  a. Add off-page connector : VR_ON
  b. Modify PU5 pinout.
  d. For +1.8VUSU OCP : modify PR22 from 4.99K to 6.2K, OCP from 3A to 3.5A
B.+VCORE:
  a.For SYSOK PULL HIGH: Stuff PR45
  b.For +VCORE sense: don't stuff PC3 & PR3 ; stuff PR51 & PR52
  c.For CPU Load line : for meet load line -1mV/A, modify PR52 & PR50 from 1K to 680 ohm
D.Charger :

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Schematic modify Item and History :

B2-->B3

1. Power -

A. Change PL11 from 4.7uH to 15uH

B. Delete PJP5

2. Design issue -

A.Correct part refence from 12 to U24

B.Change C299 part number

C.Add test points: U28, pins 1, 4, 17, 29, 36, and 37

d.Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L

e.RTC issue: VIA recommend to delete R216

1. DCON POWER -

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Schematic modify Item and History :

C1-->C2

1. Power -

A. PU6/PU7 (AOZ1021): correct the R/C of comp pin to 11K and 2.2nF

B. Change the PQ21 from CHDTC144U to ME1304AT3 (Vgs<1V)

page 27 C. Correct the +3.3VSUS to 3VPCU on PR69.1 and PR62 for prevent the +1.2V_GD glitch

D. Change the Q13 and PQ31 to AO3404 for power good giltch by +3.3V & 5V sequence issue on PU3

E. Add MAX1776 circuit for TPS62050 L/T time isn't enough.

F. Correct the +1.2V discharge circuit

page 26 G. modify the PU12.14 and connect to PQ44.3 for excessive power

page 25 H. Add R/C delay on PRE_MAIN_ON to conrtol MAIN_ON for S3 issue and reserve the D42 between MAIN_ON and PRE_MAIN_ON 3 quickly +1.2V discharge

page 24 I. Correct the Q37.2 form WL_SW to WLAN_3.3V for WLAN power sequence

J. Change the C446 to 0.47uf for prevent the giltch of WLAN_3.3V

K. Change the Q40.1 from +3.3V to WLAN_3.3V to prevent the leakage of WLAN_3.3V

page 23 L. Pull high on U28.55 for un-usd Low battery function

M. correct the R366 and R362 for EC_ID

page 21 N. SWAP the CON2.10 and CON.11

O.Add L/C on Q2.1 for DVDD_1.8V excessive noise.

page 20 P.For EMI request, change R384 to C370 & R386 to C25

Q.Change C8 to R126 for preventing no sound on speaker when S3/reboot resume.

F. Power team suggest:

1.Reserve PC123, PR164.

2.Short the PU8.2 & PU8.6 to GND for Vin_OK keep high

2. Design issue -

A.Correct part refence from 12 to U24

B.Change C299 part number

C.Add test points: U28, pins 1, 4, 17, 29, 36, and 37

d.Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L

e.RTC issue: VIA recommend to delete R216

1. DCON POWER -

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Schematic modify Item and History :

C2-->C3

1. *Boot problems:*
   PR31 : 22ohm -> 10ohm. (10 ohm is normal value.)

2. *Flash problems:*
   Add pull-up resistor R396 (4.7k 0402).

3. *Very loud whining when connected to a solar panel*
   Relpace PD22 to schottky diode and invert it (the cathode of PD22 connect to PR152/PC102).
   PC102 - 0.47uF, 6V, 0402, Y7V
   PR116 - 475K, 1%, 0402
   PR117 - 28K, 1%, 0402
   PR120 - 28K, 1%, 0402
   PR125 - 2.2K, 5%, 0402
   PR126 - 2.2K, 5%, 0402
   PR144 - 330K, 1%, 0402

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