CL1B Block Diagram

C2
2009-12-30

VTERM(+0.9V)
VTT(+1.05V)
+1.5VSUS
+1.5V
+1.8VMEM
+1.8V
+2.5V
3VPCU
+3.3V
+3.3VSUS
LCD_3.3V
LCD_5V
+5V

C7-M (ULV)

VCORE:+1.196 ~ +0.748
VCCP:+1.05V
VCCA:+1.8V or +1.5V

VID[0:6] → CPU VCORE

+/- CPU_CLK
+/- HCLK → Clock Gengerator ICS9UM7002

V4 BUS

Frame Buffer

7" LCD — DCON

VX855(U)

VTT:VCCP (+1.05V)
VCC15:+1.5V or +1.2V
VCC33:+3.3V
VCCMEM:+1.8V
VSUS15:+1.5VSUS
VSUS33:+3.3VSUS

CHA → DDRII 1GB

SDIO I/F → MICRO SD

VIP I/F → Camera

SDIO I/F → WLAN Conn. → WLAN Module

WLAN Conn. → Card Reader SD Card SLOT

USB → USB PORT X3

LPC BUS → EC KB3700

EC KB3700 → SPI Flash

EC KB3700 → Int. KB

EC KB3700 → T/P

EC KB3700 → Battery → Charger

HD Audio

HDA CODEC CX20582 — Int. SPK

HDA CODEC CX20582 — Audio Jack

HDA CODEC CX20582 — Int. Mic

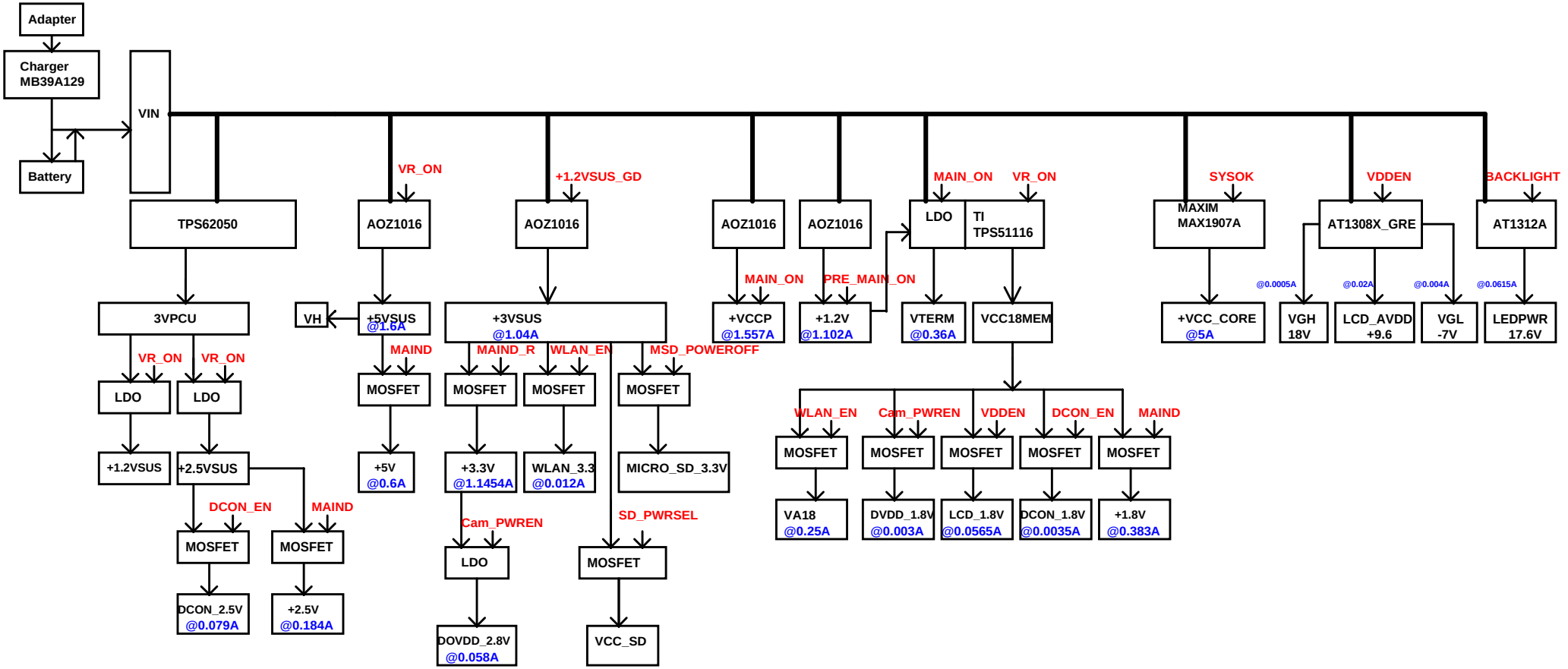
Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	BLOCK DIAGRAM	3A

Date: Monday, March 15, 2010 Sheet 1 of 36

Power Seides

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	S5	S3	S1	S0
VIN	+3.0~+20V	MAIN power		V	V	V	V
VCCRTC_1	+3.0V~+3.3V	RTC		V	V	V	V
SVP3Cp	+3.3V	EC power	ALWON	V	V	V	V
+1.2VSUS	+1.2V	Suspend power	SVP3Cp	V	V	V	S
+5VSUS	+5V	Suspend power	VR_ON	V	V	V	S
VA	+5V	+5Vdual power set gate power	VR_ON	V	V	V	S
+3VSUS	+3.3V	Suspend power	+1.2VSUS_EC	V	V	V	S
VCC1394EM	+1.8V	Mini-cry power	VR_ON	V	V	V	S
VTERM	+0.9V	Mini-cry power	MAIN_ON	V	V	S	S
+1.2V	+1.2V	VGBIOS core power	PRE_MAIN_ON(SUSB#)	V	V	S	S
+5V	+5V	Audio power	MAIN3	V	S	S	S
+3.3V	+3.3V	Clock gen/CPU Clock PLL/VGA I/O power/CRC/Modulin power	MAIN_S_R	V	S	S	S
+3.3V	+3.3V	LVDS and LVDS CPU power	MAIN3	V	S	S	S
VCCP	+1.05V	I/O power for R-net interface/ I/O power for CPU signals	MAIN_ON	V	S	S	S
+VCC_CORE	0.7500~+1.550	CPU core power	SYSON	V	S	S	S
WLAN_3.3V	+3.3V	WLAN power	WLAN_EN	V	S	S	S
VCC_SD	+3.3V	SD power	SD_PWRDRP	V	S	S	S
MICRO_SD_3.3V	+3.3V	Micro SD power	MSD_PWRDPP	V	S	S	S
LCD_AVDD	+8.6V	Analog power for LCD	SDSEN	V	S	S	S
VGH	+16V	TFT on power for LCD	+5V_EN	V	S	S	S
VBL	-7V	TFT off power for LCD	LCD_AVDD	V	S	S	S
+1.8V	+1.8V	Digital power of LCD/CPU PLL power	LCD_AVDD	V	S	S	S
VBAT	+6V~+13V	MAIN BATTERY	CHG	V	V	V	V

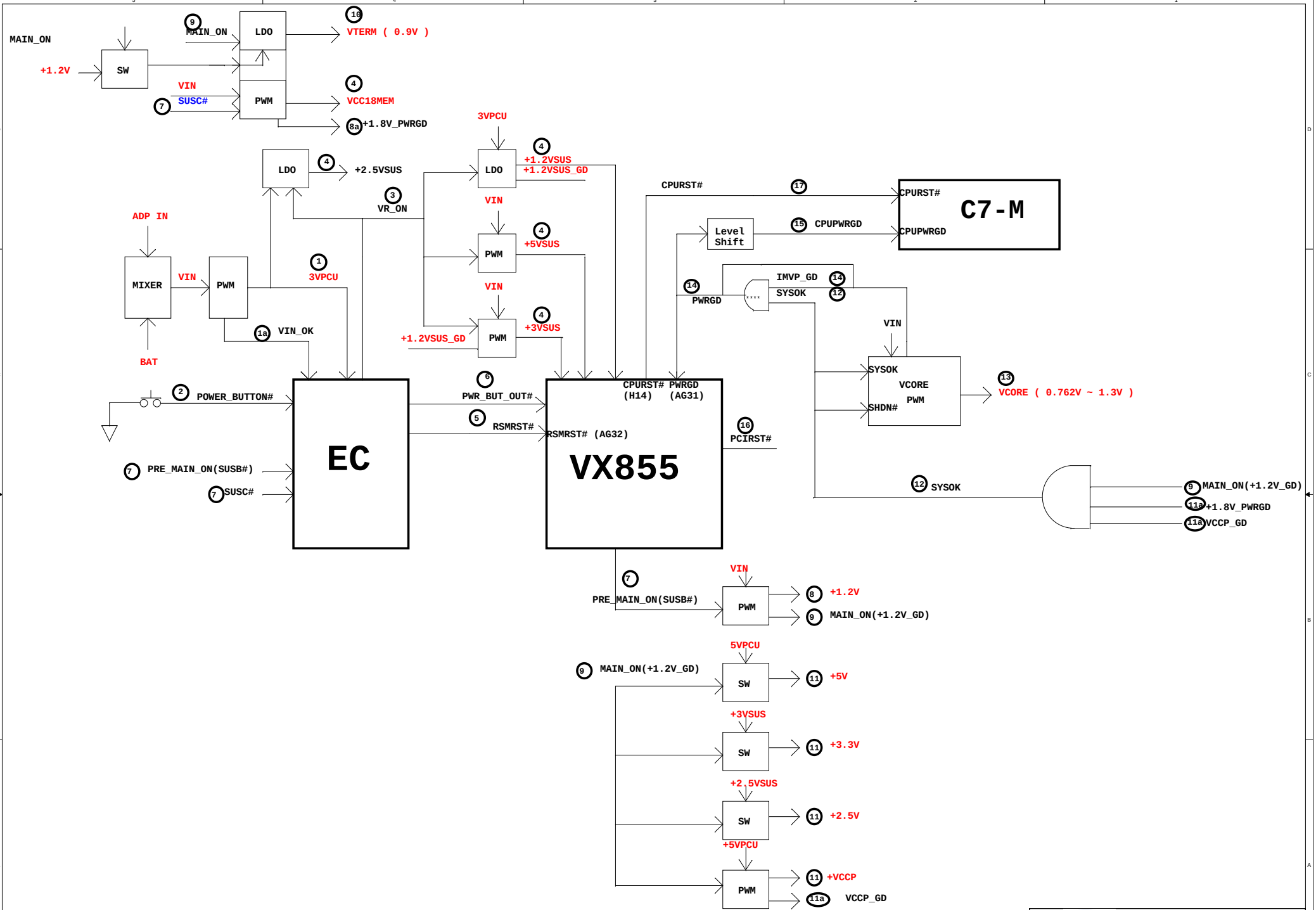


Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	POWER MANGER DIAGRAM	3A

Date: Monday, March 15, 2010 Sheet 2 of 36

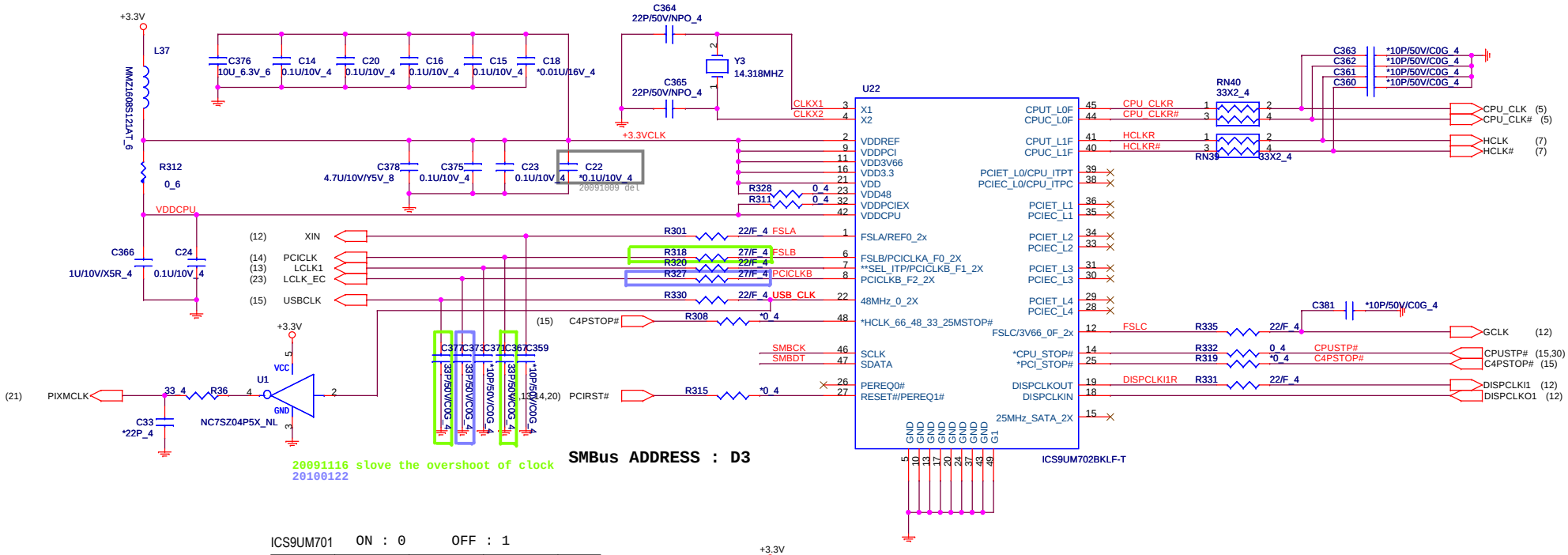


Quanta Computer Inc.

PROJECT : CL1B

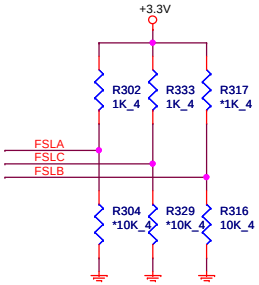
Size	Document Number	Rev
	Power Sequency	3A

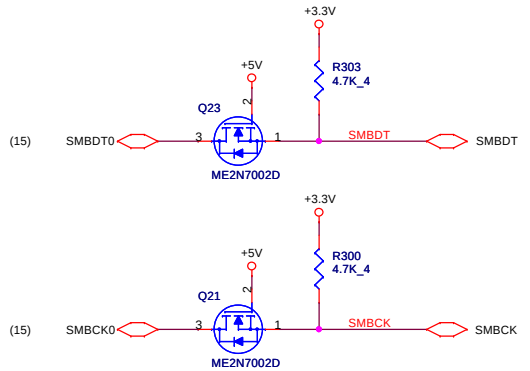
Date: Monday, March 15, 2010 Sheet 3 of 36



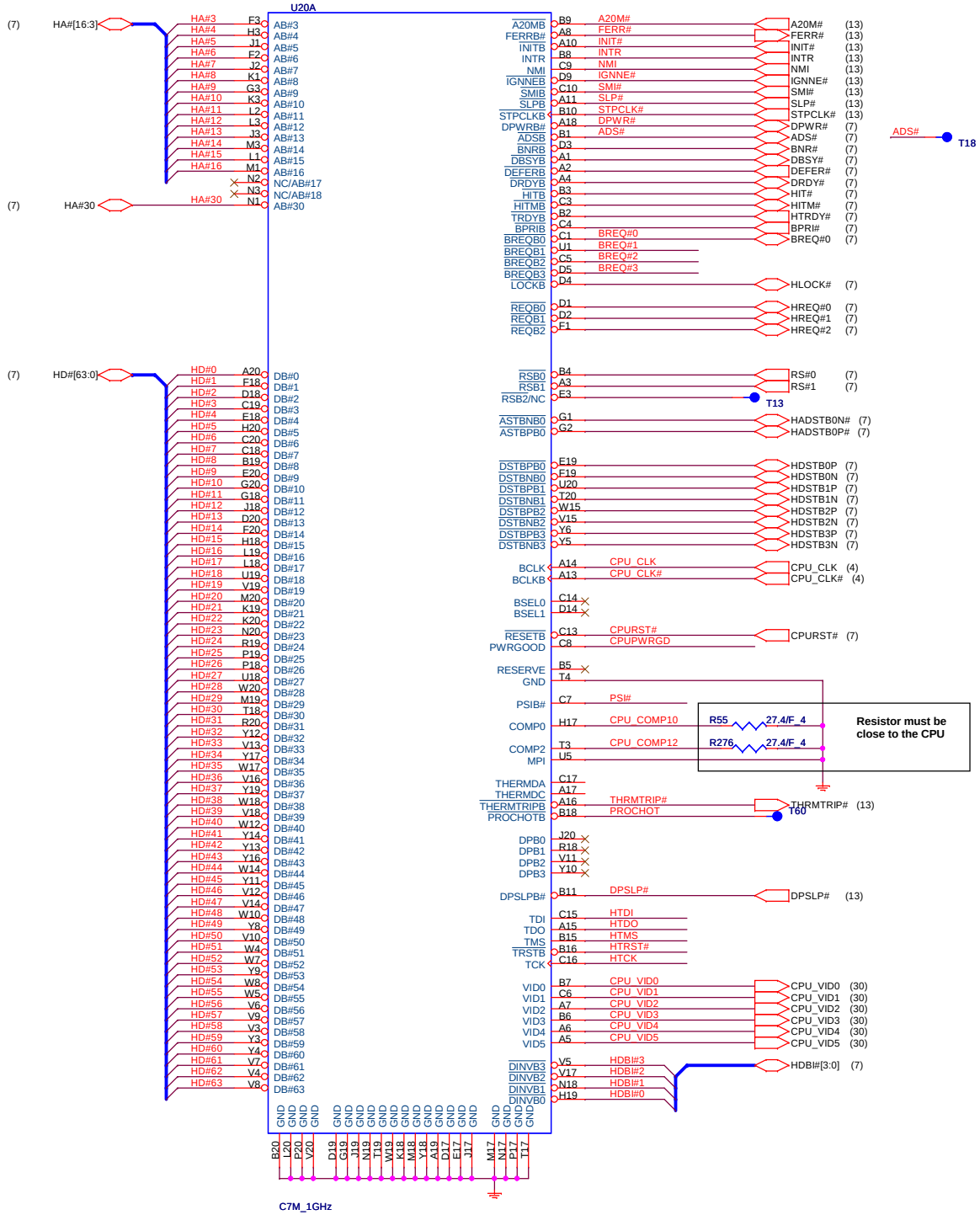
ICS9UM701 ON : 0 OFF : 1

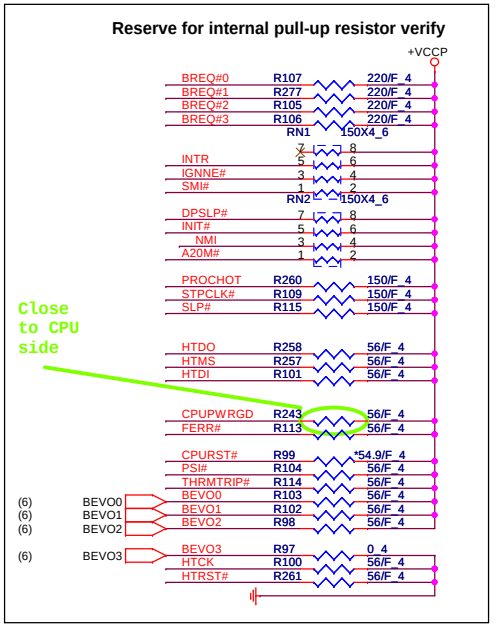
3	2	1		
FSLA	FSLC	FSLB	CPU	PCI
0	0	0	266.66	33
1	0	0	133.33	33
0	0	1	200	33
1	0	1	166.66	33
0	1	0	333.33	33
1	**1**	**0**	**100**	33
0	1	1	400	33
1	**1**	**1**	**200**	33

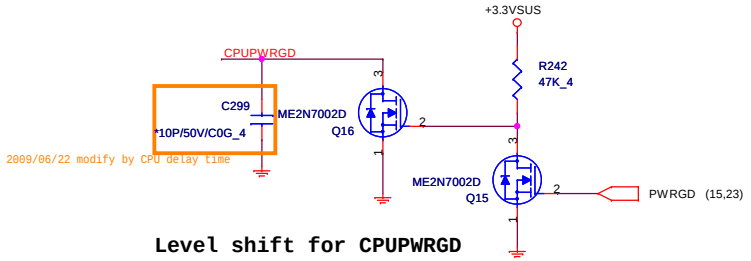




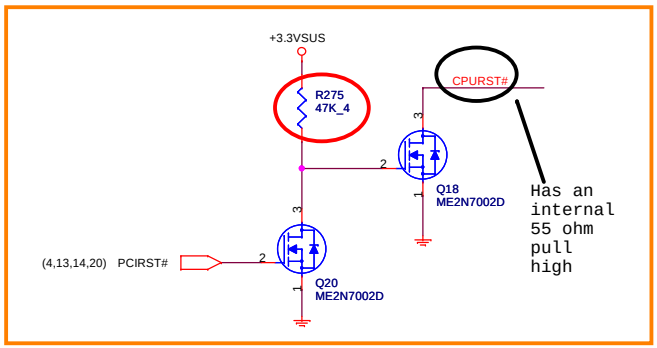
Quanta Computer Inc.			
PROJECT : CL1B			
Size	Document Number		Rev
	CLOCK GENERATOR		3A
Date: Monday, March 15, 2010		Sheet 4 of 36	



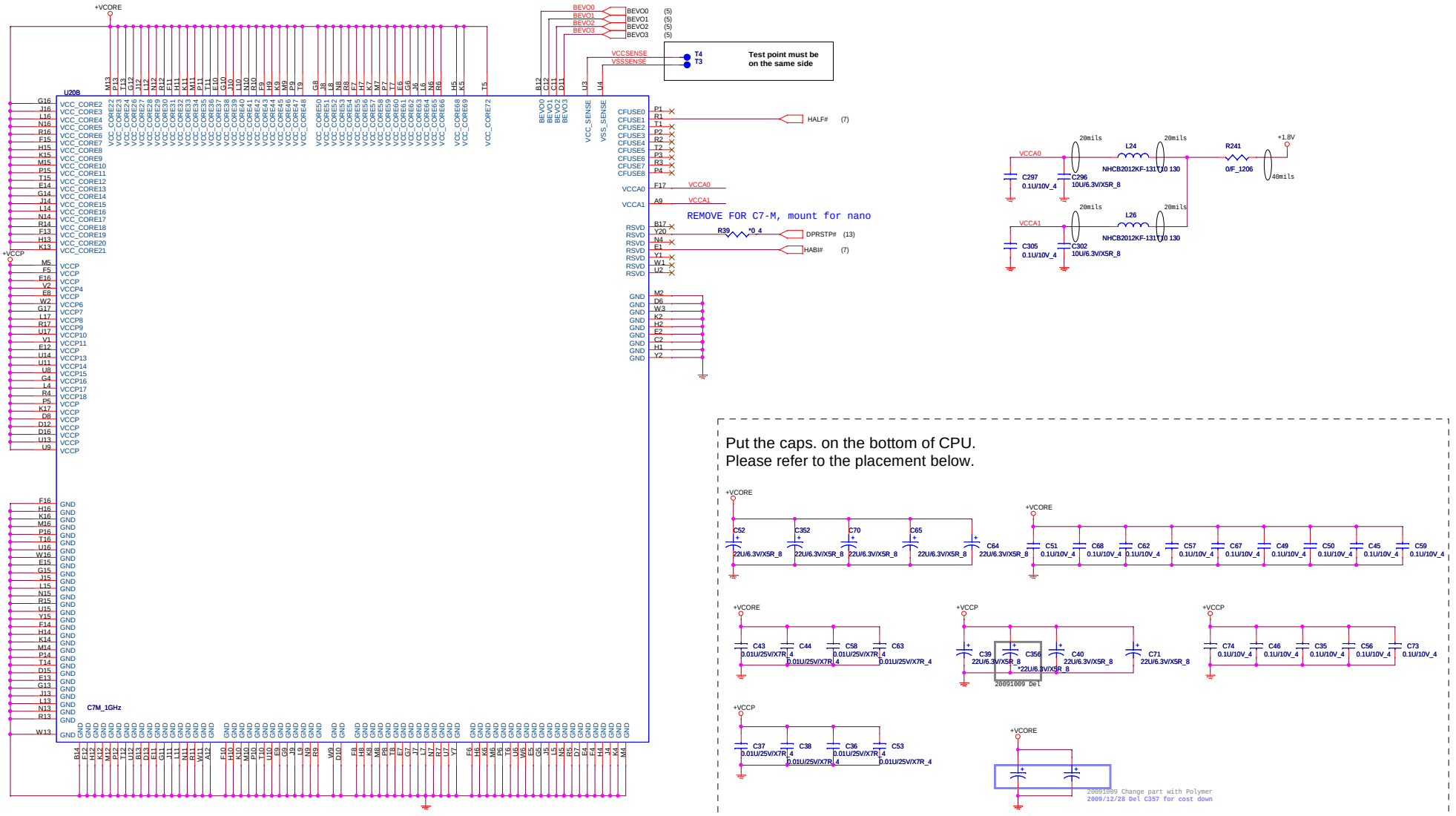




Level shift for CPUPWRGD



Quanta Computer Inc.			
PROJECT : CL1B			
Size	Document Number		Rev
	CPU C7M V4BUS		3A
Date: Monday, March 15, 2010		Sheet 5 of 36	



Put the caps. on the bottom of CPU.
Please refer to the placement below.

Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	CPU C7M POWER&GND	3A
Date: Monday, March 15, 2010	Sheet 6 of 36	

+3.3V

L28
NHCB2012KF-131T10 130

20091116 Delete 0 ohm

C321
4.7U/10V/Y5V_8

C98
0.1U/10V_4

C91
1000P/50V/X7R_4

VCCA33HCK

+VCCP

U19A

J15

L12 L14 L16 L18 M11 M13 M15 M17 N12 N14 N16

VTT

VCCA33HCK

(4) HCLK
(4) HCLK#

HCLK
HCLK#

J12 HCLK+
J13 HCLK-

(5) HA#[16:3]

HA#3 E16 HA3
HA#4 G18 HA4
HA#5 H20 HA5
HA#6 H21 HA6
HA#7 G19 HA7
HA#8 E20 HA8
HA#9 F17 HA9
HA#10 G20 HA10
HA#11 D21 HA11
HA#12 A21 HA12
HA#13 F21 HA13
HA#14 E21 HA14
HA#15 B21 HA15
HA#16 G22 HA16

(5) HA#30 H22 HAHI0

(6) HABI#
(6) HALF#

R122 *0_4
R233 *0_4

D17 HABI
F18 HALF

HOST
Rev0.2

(5) CPURST# H14 CPURST
(5) ADS# H18 HADS
(5) BNR# H13 HBNR
(5) BPRI# E12 HBPRI
(5) DBSY# H17 HDBSY
(5) DEFER# G15 HDEFER
(5) DRDY# C12 HDRDY
(5) HIT# F15 HHIT
(5) HITM# G14 HHITM
(5) HLOCK# F14 HLOCK

(5) HREQ#0
(5) HREQ#1
(5) HREQ#2

HREQ#0 D16 HREQ0
HREQ#1 C16 HREQ1
HREQ#2 E17 HREQ2

(5) HTRDY# C15 HTRDY

(5) RS#0 D12 HRS0
(5) RS#1 E15 HRS1

(5) BREQ#0 G16 HBREQ0

HDB#0 A12 HDBI0
HDB#1 B11 HDBI1
HDB#2 H8 HDBI2
HDB#3 G4 HDBI3

(5) HDBI#[3:0]

(5) HADSTB0N#
(5) HADSTB0P#

F19 HADSTB0N
E19 HADSTB0P

(5) DPWR# F13 HDPWR

DPWR#

GNDA33HCK

J14

VX855_27x27_08M

HD0 B15 HD#0
HD1 B13 HD#1
HD2 E11 HD#2
HD3 C14 HD#3
HD4 G12 HD#4
HD5 F11 HD#5
HD6 G11 HD#6
HD7 C11 HD#7
HD8 A15 HD#8
HD9 B14 HD#9
HD10 H12 HD#10
HD11 A11 HD#11
HD12 G10 HD#12
HD13 D10 HD#13
HD14 A13 HD#14
HD15 F10 HD#15
HD16 C10 HD#16
HD17 D9 HD#17
HD18 C7 HD#18
HD19 B6 HD#19
HD20 A9 HD#20
HD21 C8 HD#21
HD22 B10 HD#22
HD23 A8 HD#23
HD24 H9 HD#24
HD25 E9 HD#25
HD26 F9 HD#26
HD27 E8 HD#27
HD28 C6 HD#28
HD29 B9 HD#29
HD30 H10 HD#30
HD31 D8 HD#31
HD32 C2 HD#32
HD33 E7 HD#33
HD34 B5 HD#34
HD35 C3 HD#35
HD36 D6 HD#36
HD37 A5 HD#37
HD38 E7 HD#38
HD39 G8 HD#39
HD40 B1 HD#40
HD41 D5 HD#41
HD42 B2 HD#42
HD43 C4 HD#43
HD44 A4 HD#44
HD45 E5 HD#45
HD46 G7 HD#46
HD47 F6 HD#47
HD48 D4 HD#48
HD49 E3 HD#49
HD50 D2 HD#50
HD51 G2 HD#51
HD52 F3 HD#52
HD53 F1 HD#53
HD54 D1 HD#54
HD55 E5 HD#55
HD56 H6 HD#56
HD57 H5 HD#57
HD58 G3 HD#58
HD59 H1 HD#59
HD60 H2 HD#60
HD61 G6 HD#61
HD62 H4 HD#62
HD63 E4 HD#63

HD#[63:0] (5)

HDSTB0P D14 HDSTB0P (5)
HDSTB0N D13 HDSTB0N (5)

HDSTB1P A7 HDSTB1P (5)
HDSTB1N B7 HDSTB1N (5)

HDSTB2P B3 HDSTB2P (5)
HDSTB2N A3 HDSTB2N (5)

HDSTB3P F2 HDSTB3P (5)
HDSTB3N F1 HDSTB3N (5)

HGTLVREF0
HGTLVREF1

J21
J18

GTLVREF

HGTLPVT_REXT

J17 HGTLPVT_REXT R236 54.9/F_4

Place VX855Bottom

+VCCP

C319 4.7U/10V/Y5V_8
C315 4.7U/10V/Y5V_8
C307 1U/10V/X5R_6
C311 1U/10V/X5R_6
C95 0.01U/25V/X7R_4
C102 1000P/50V/X7R_4

Debug test point

HD#48 1 HD1
HD#24 1 HD3
HD#33 1 HD2

2/3 of VCCP +/-2%

R116 49.9/F_4

+VCCP

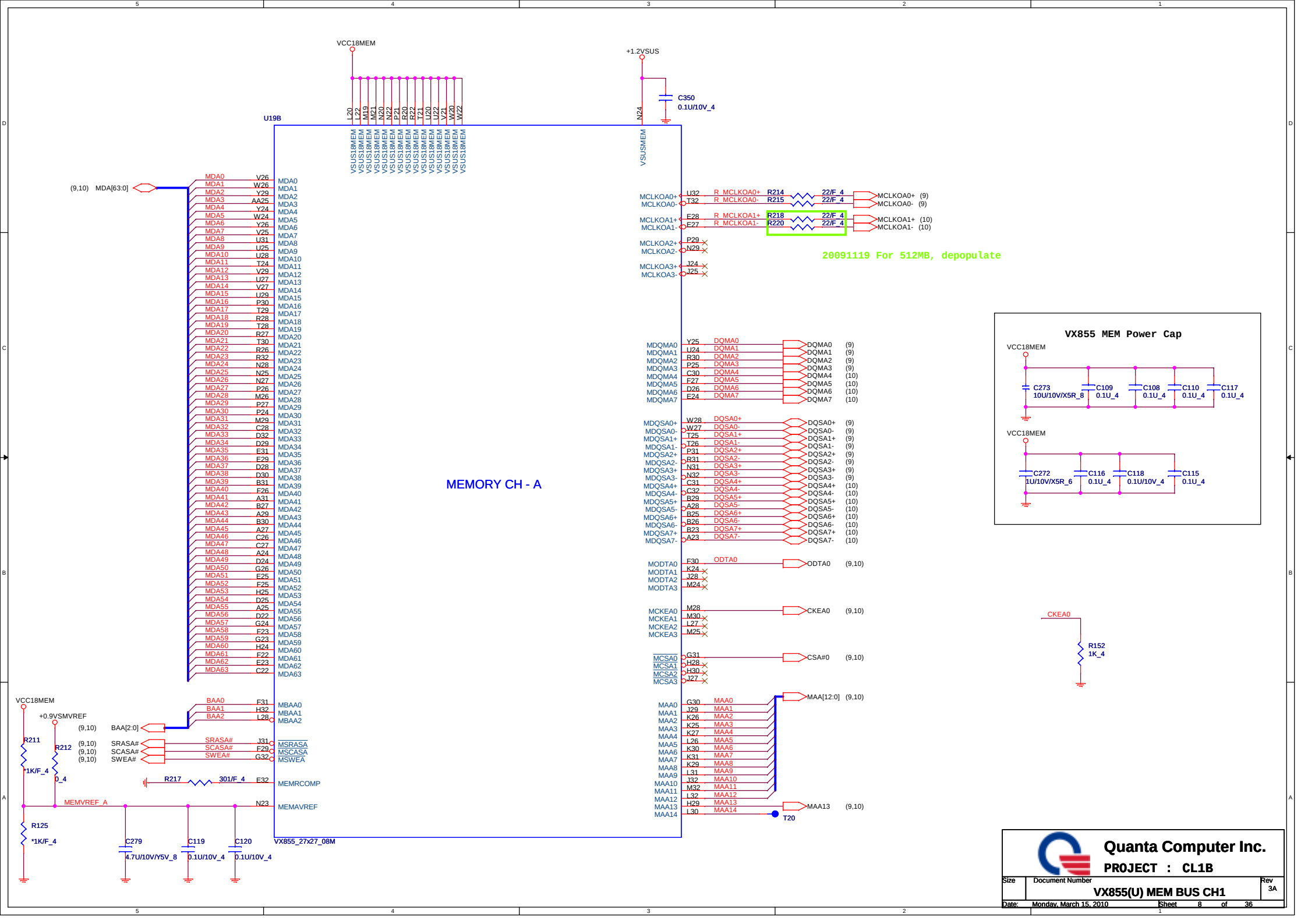
C111 0.1U/10V_4
C114 0.1U/10V_4
C106 0.1U/10V_4

R118 100/F_4

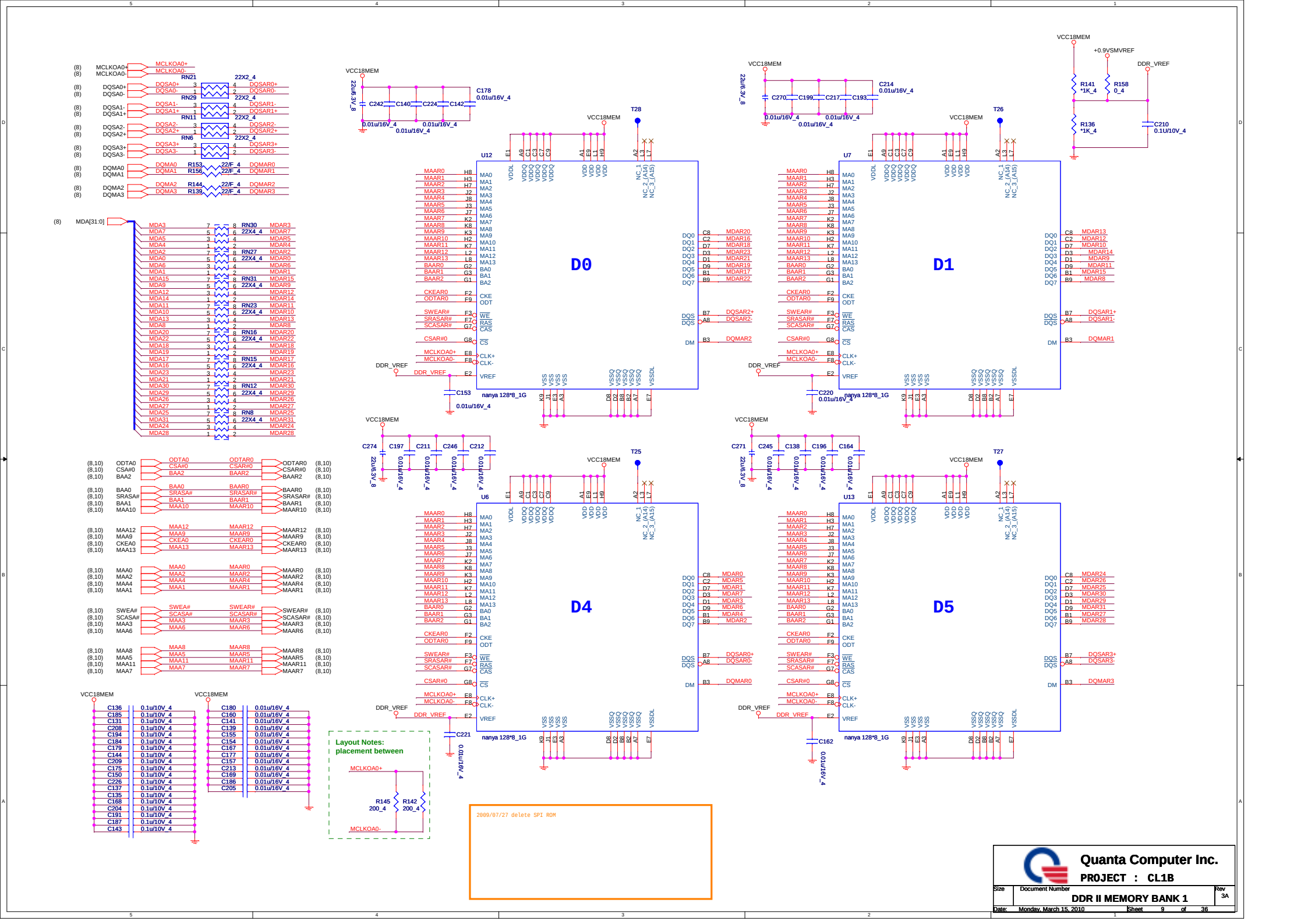
Quanta Computer Inc.
PROJECT : CL1B

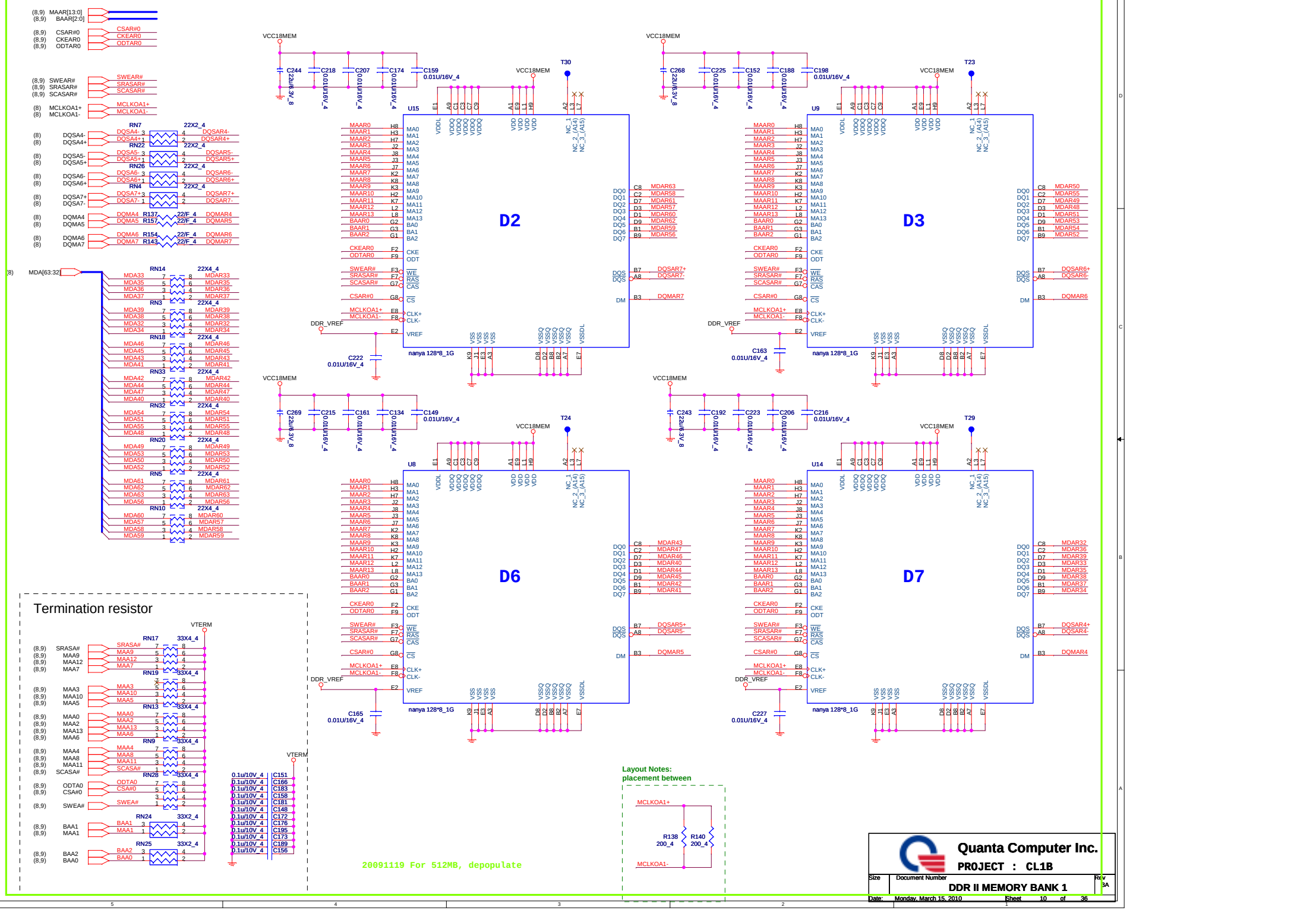
Size	Document Number	Rev
	VX855(U) HOST BUS	3A

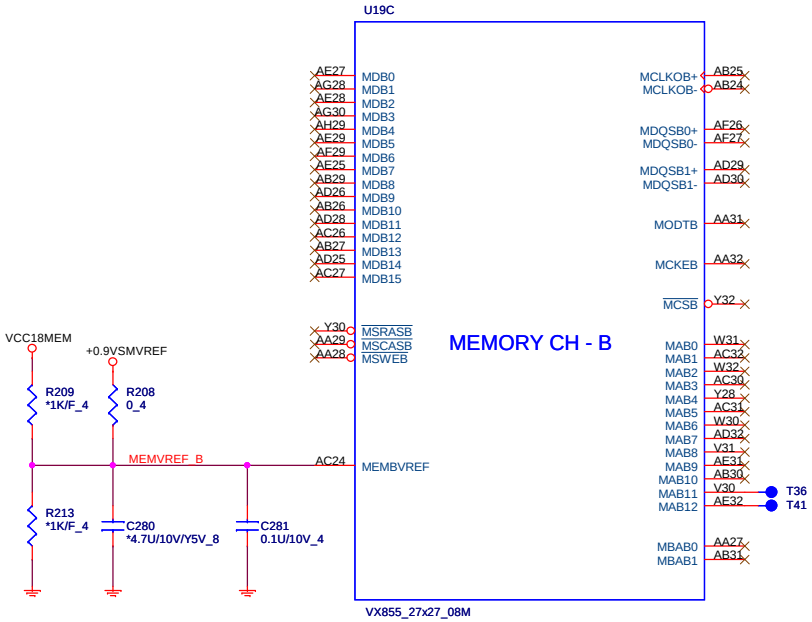
Date: Monday, March 15, 2010 Sheet 7 of 36



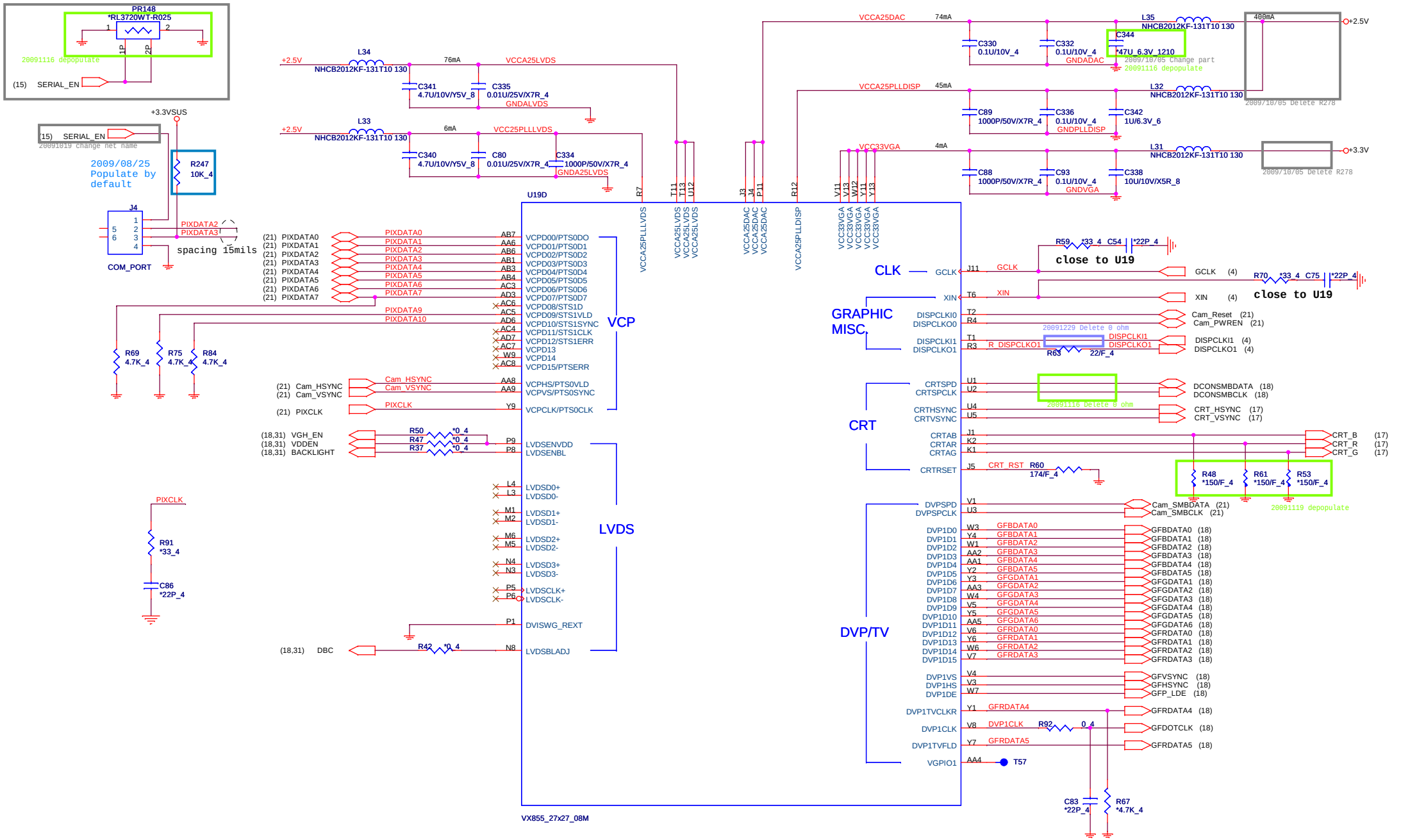
Quanta Computer Inc.			
PROJECT : CL1B			
Size	Document Number		Rev
	VX855(U) MEM BUS CH1		3A
Date: Monday, March 15, 2010		Sheet 8 of 36	


D0
D1
D4
D5
U12
U7
U6
U13
T28
T26
T25
T27
VCC18MEM
+0.9VSMVREF
DDR_VREF
nanya 128*8_1G
Layout Notes:
placement between
2009/07/27 delete SPI ROM
Quanta Computer Inc.
PROJECT : CL1B
DDR II MEMORY BANK 1
Size
Document Number
Rev
3A
Date: Monday, March 15, 2010
Sheet 9 of 36


D2
D3
D6
D7
U15
U9
U8
U14
T30
T23
T24
T29
nanya 128*8_1G
VCC18MEM
DDR_VREF
MAA[13:0]
BAA[2:0]
CSA#0
CKEA0
ODTA0
SWEA#
SRASA#
SCASA#
MCLKOA1+
MCLKOA1-
DQSA4-
DQSA4+
DQSA5-
DQSA5+
DQSA6-
DQSA6+
DQSA7+
DQSA7-
DQMA4
DQMA5
DQMA6
DQMA7
MDA[63:32]
Termination resistor
VTERM
20091119 For 512MB, depopulate
Layout Notes:
placement between
R138
200_4
R140
200_4
Quanta Computer Inc.
PROJECT : CL1B
DDR II MEMORY BANK 1
Size
Document Number
Rev
3A
Date: Monday, March 15, 2010
Sheet 10 of 36



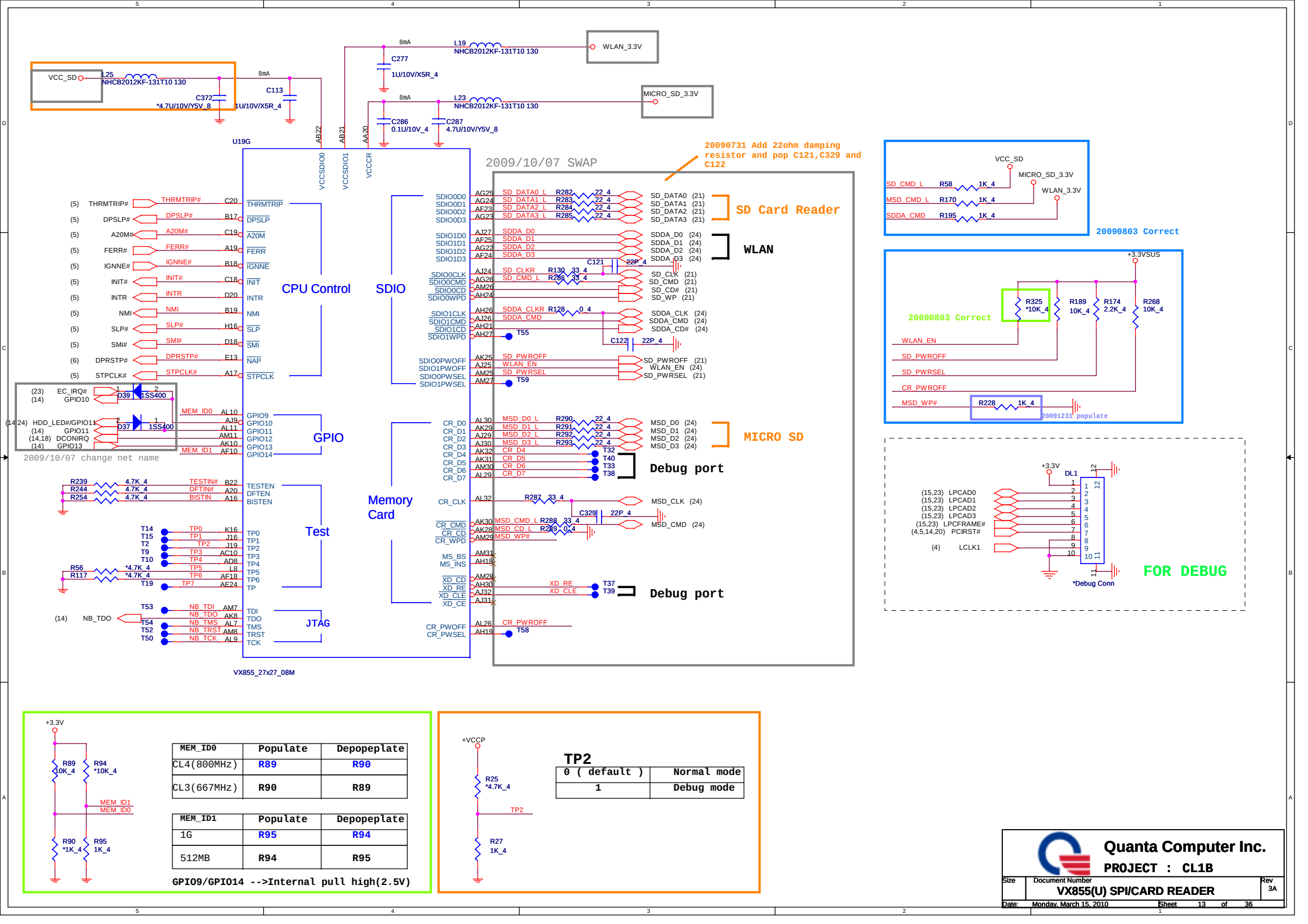
Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number: VX855(U) MEM BUS CH2 & PCIE	Rev 3A
Date: Monday, March 15, 2010	Sheet 11 of 36	



Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) VIDEO BUS	3A
Date: Monday, March 15, 2010	Sheet 12 of 36	



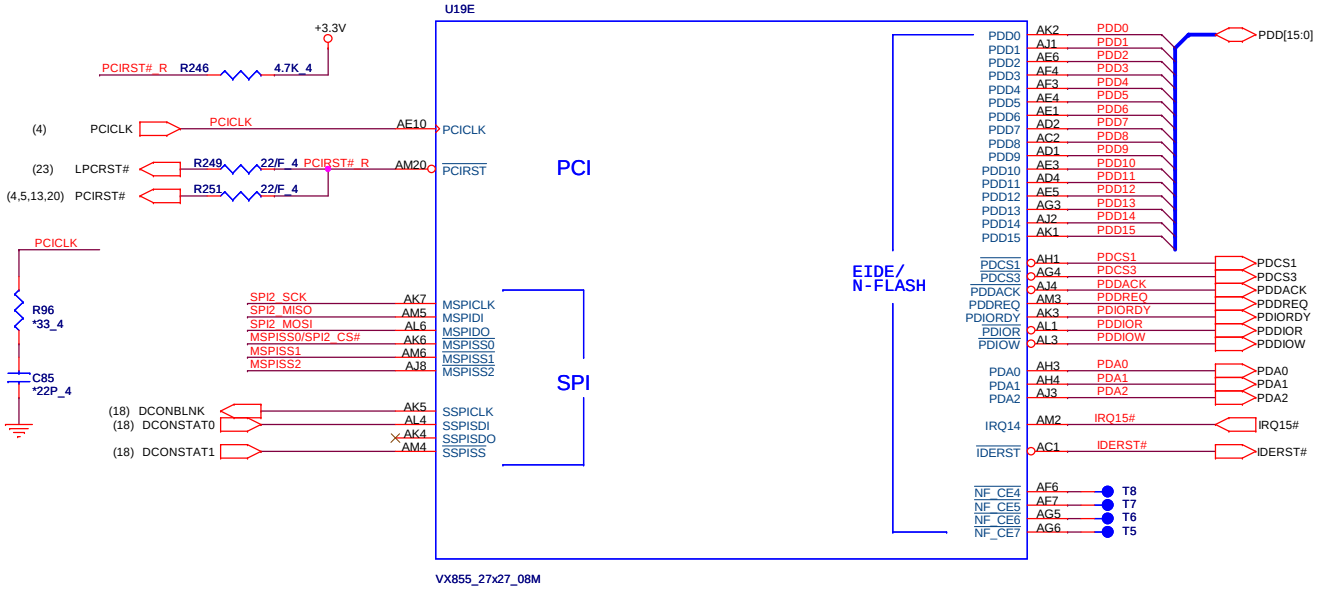
MEM_ID0	Populate	Depopeplate
CL4(800MHz)	R89	R90
CL3(667MHz)	R90	R89

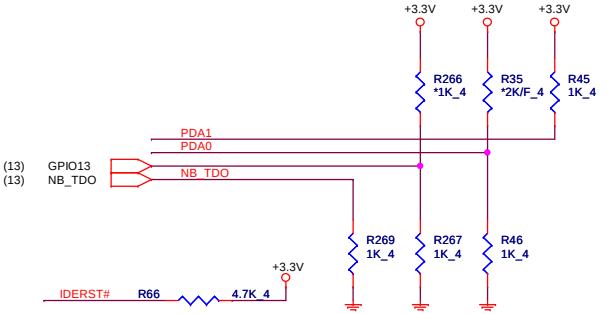
MEM_ID1	Populate	Depopeplate
1G	R95	R94
512MB	R94	R95

Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) SPI/CARD READER	3A

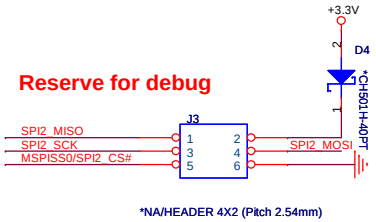
Date: Monday, March 15, 2010 Sheet 13 of 36

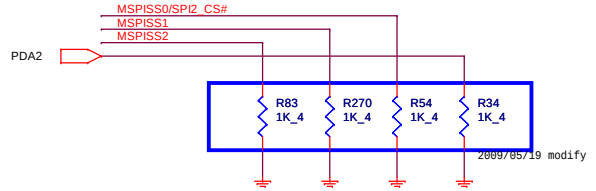


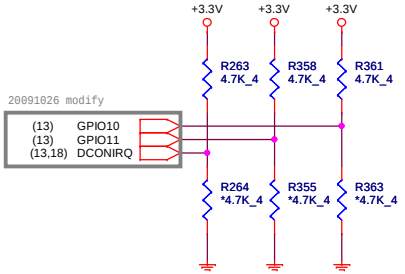


NB Strapping

Pin	Function	Pull Low	Pull High
PDA1	PLL OK source select	from NB PLL	from SB Logic*
PDA0	IOQ depth	12 *	1
GPIO13	GTL pull up	Enable *	Disable
NB_TDO	Debug Link enable	XD Mode*	Debug Link

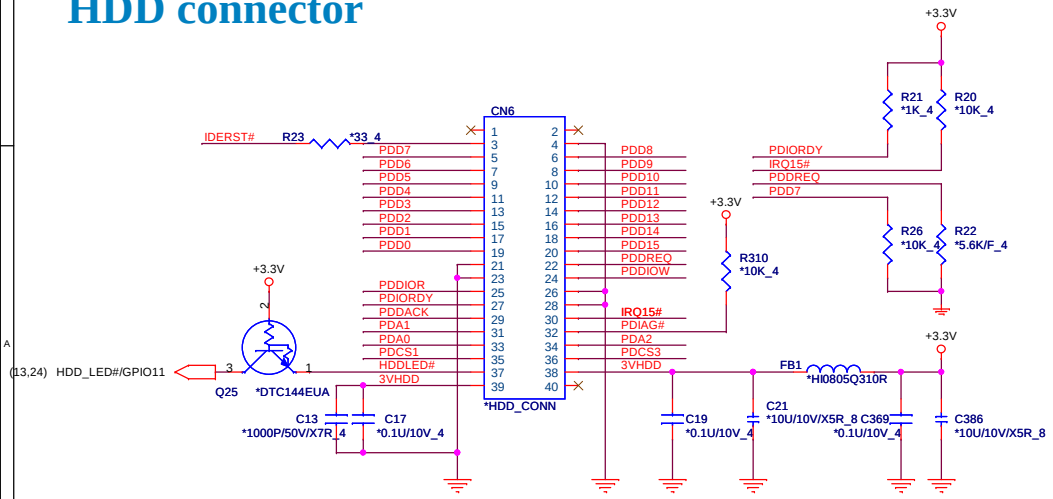






2009/10/01 don't populate

HDD connector



SB Strapping

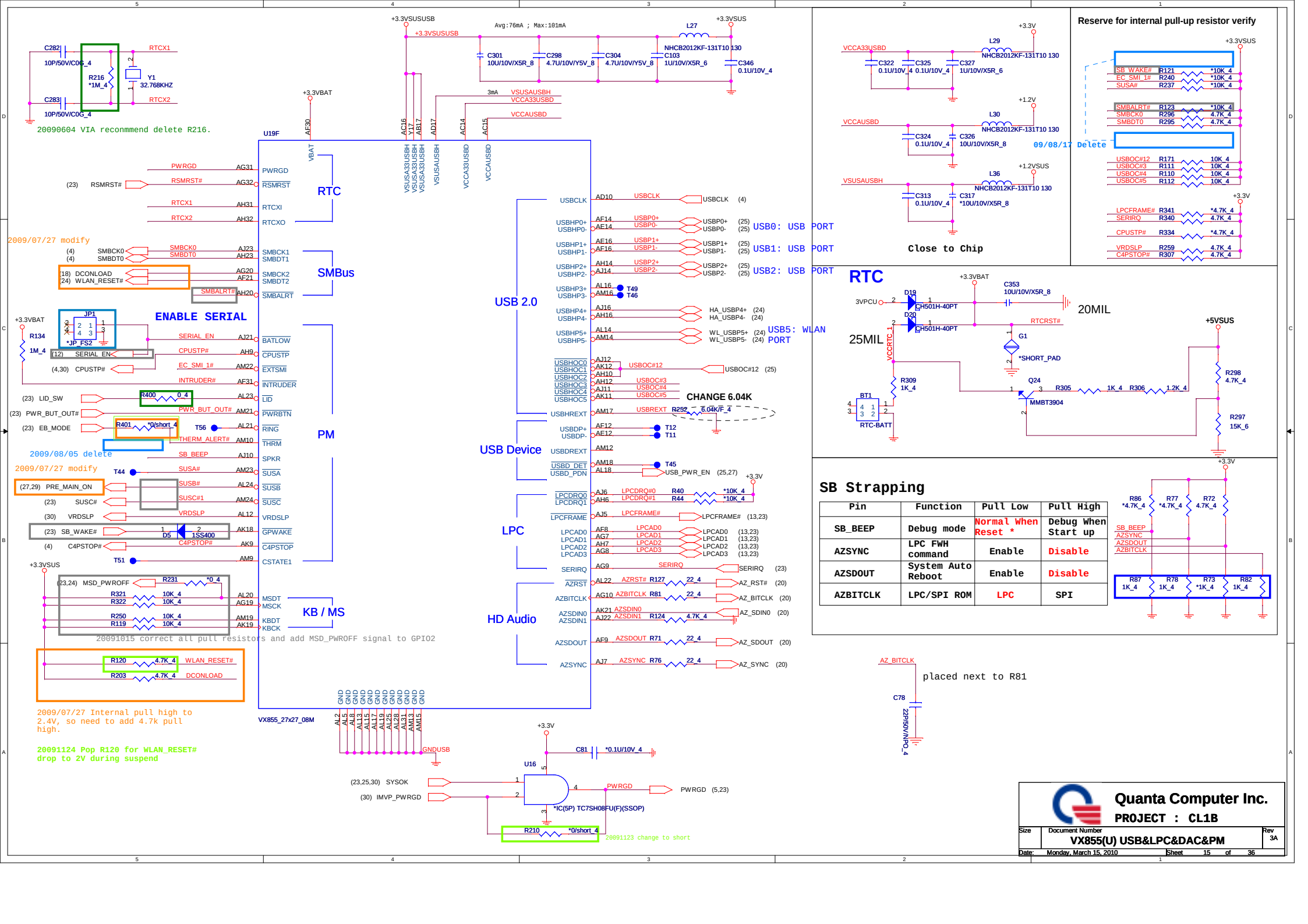
Pin	0:LOW 1:High	Function
MSPISS1/ MSPISS0	00*	IDE
	01	NFC
	10	CE ATA
MSPISS2	0: SPI/LPC *	NFC ROM Select
	1: NFC ROM	
PDA2	0: Disable *	PCI Master Mode Enable
	1: Enable	

NB Strapping

Pin	0:Low 1:High	FSB Freq.
GPIO12/ GPIO11/ GPIO10	000	100Mhz
	001	133Mhz
	010	200Mhz
	011	266Mhz
	111 *	Auto Mode

Quanta Computer Inc.
PROJECT : CL1B

Size	Document Number	Rev
	VX855(U) PCI&PATA&SATA BUS	3A
Date: Monday, March 15, 2010	Sheet 14 of 36	


C282 10P/50V/C0G_4
C283 10P/50V/C0G_4
R216 *1M_4
Y1 32.768KHZ
RTCX1
RTCX2
20090604 VIA reconmmend delete R216.
+3.3VSUSUSB
Avg:76mA ; Max:101mA
L27
NHCB2012KF-131T10 130
C301 10U/10V/X5R_8
C298 4.7U/10V/Y5V_8
C304 4.7U/10V/Y5V_8
C103 1U/10V/X5R_6
C346 0.1U/10V_4
+3.3VSUS
+3.3VBAT
3mA
VSUSAUSBH
VCCA33USBD
VCCAUSBD
U19F
VBAT
RTC
PWRGD
RSMRST#
RTCXI
RTCXO
2009/07/27 modify
SMBCK0
SMBDT0
SMBCK1
SMBDT1
SMBCK2
SMBDT2
SMBALRT#
SMBus
DCONLOAD
WLAN_RESET#
ENABLE SERIAL
JP1
*JP_FS2
SERIAL_EN
CPUSTP#
EC_SMI_1#
INTRUDER#
LID_SW
PWR_BUT_OUT#
EB_MODE
R400 0_4
R401 *0/short_4
T56
THERM_ALERT#
2009/08/05 delete
SB_BEEP
2009/07/27 modify
T44
SUSA#
SUSB#
SUSC#
VRDSLP
SB_WAKE#
C4PSTOP#
T51
CSTATE1
PM
BATLOW
CPUSTP
EXTSMI
INTRUDER
LID
PWRBTN
RING
THRM
SPKR
SUSA
SUSB
SUSC
VRDSLP
GPWAKE
C4PSTOP
+3.3VSUS
MSD_PWROFF
R231 *0_4
R321 10K_4
R322 10K_4
R250 10K_4
R119 10K_4
MSDT
MSCK
KBDT
KBCK
KB / MS
20091015 correct all pull resistors and add MSD_PWROFF signal to GPIO2
R120 4.7K_4
R203 4.7K_4
WLAN_RESET#
DCONLOAD
2009/07/27 Internal pull high to 2.4V, so need to add 4.7k pull high.
20091124 Pop R120 for WLAN_RESET# drop to 2V during suspend
VX855_27x27_08M
GNDUSB
USB 2.0
USBCLK
USBP0+
USBP0-
USB0: USB PORT
USBP1+
USBP1-
USB1: USB PORT
USBP2+
USBP2-
USB2: USB PORT
USBP3+
USBP3-
T49
T46
USBP4+
USBP4-
HA_USBP4+
HA_USBP4-
USBP5+
USBP5-
WL_USBP5+
WL_USBP5-
USB5: WLAN PORT
USBOC#12
USBOC#3
USBOC#4
USBOC#5
CHANGE 6.04K
USBREXT
R252 6.04K/F_4
USB Device
USBDP+
USBDP-
T12
T11
USBDREXT
USBD_DET
USBD_PDN
T45
USB_PWR_EN (25,27)
LPC
LPCDRQ0
LPCDRQ1
LPCDRQ#0
LPCDRQ#1
R40 *10K_4
R44 *10K_4
LPCFRAME#
LPCAD0
LPCAD1
LPCAD2
LPCAD3
SERIRQ
HD Audio
AZRST#
AZBITCLK
R127 22_4
R81 22_4
AZSDIN0
AZSDIN1
R124 4.7K_4
AZSDOUT
R71 22_4
AZSYNC
R76 22_4
AZ_RST# (20)
AZ_BITCLK (20)
AZ_SDIN0 (20)
AZ_SDOUT (20)
AZ_SYNC (20)
U16
C81 *0.1U/10V_4
SYSOK
IMVP_PWRGD
PWRGD (5,23)
*IC(5P) TC7SH08FU(F)(SSOP)
R210 *0/short_4
20091123 change to short
VCCA33USBD
L29
NHCB2012KF-131T10 130
C322 0.1U/10V_4
C325 0.1U/10V_4
C327 1U/10V/X5R_6
VCCAUSBD
L30
C324 0.1U/10V_4
C326 10U/10V/X5R_8
09/08/17 Delete
VSUSAUSBH
L36
C313 0.1U/10V_4
C317 *10U/10V/X5R_8
Close to Chip
Reserve for internal pull-up resistor verify
SB_WAKE# R121 *10K_4
EC_SMI_1# R240 *10K_4
SUSA# R237 *10K_4
SMBALRT# R123 *10K_4
SMBCK0 R296 4.7K_4
SMBDT0 R295 4.7K_4
USBOC#12 R171 10K_4
USBOC#3 R111 10K_4
USBOC#4 R110 10K_4
USBOC#5 R112 10K_4
LPCFRAME# R341 *4.7K_4
SERIRQ R340 4.7K_4
CPUSTP# R334 *4.7K_4
VRDSLP R259 4.7K_4
C4PSTOP# R307 4.7K_4
RTC
3VPCU
D19 CH501H-40PT
D20 CH501H-40PT
C353 10U/10V/X5R_8
20MIL
25MIL
VCCRTC_1
RTCRST#
G1
*SHORT_PAD
+5VSUS
R309 1K_4
BT1
RTC-BATT
Q24
MMBT3904
R305 1K_4
R306 1.2K_4
R298 4.7K_4
R297 15K_6
SB Strapping
Pin | Function | Pull Low | Pull High
SB_BEEP | Debug mode | Normal When Reset * | Debug When Start up
AZSYNC | LPC FWH command | Enable | Disable
AZSDOUT | System Auto Reboot | Enable | Disable
AZBITCLK | LPC/SPI ROM | LPC | SPI
R86 *4.7K_4
R77 *4.7K_4
R72 4.7K_4
R87 1K_4
R78 1K_4
R73 *1K_4
R82 1K_4
AZ_BITCLK
placed next to R81
C78 22P/50V/NPO_4
Quanta Computer Inc.
PROJECT : CL1B
Size
Document Number
VX855(U) USB&LPC&DAC&PM
Rev 3A
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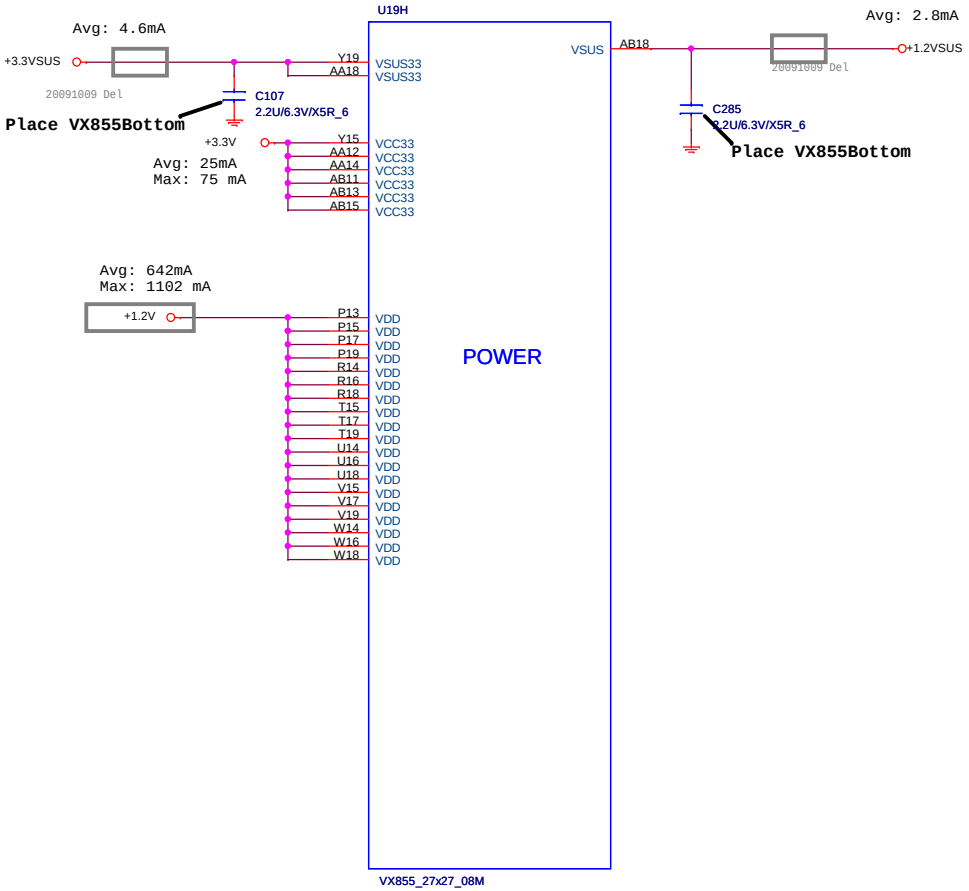

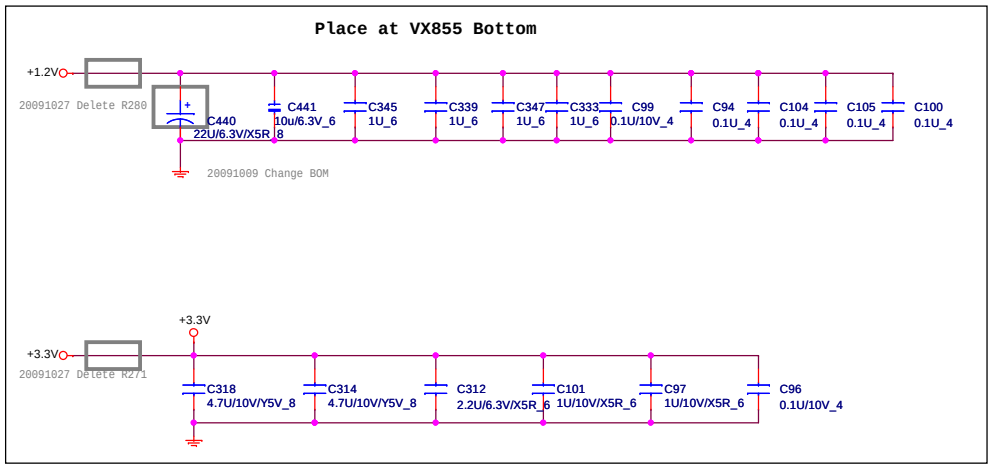

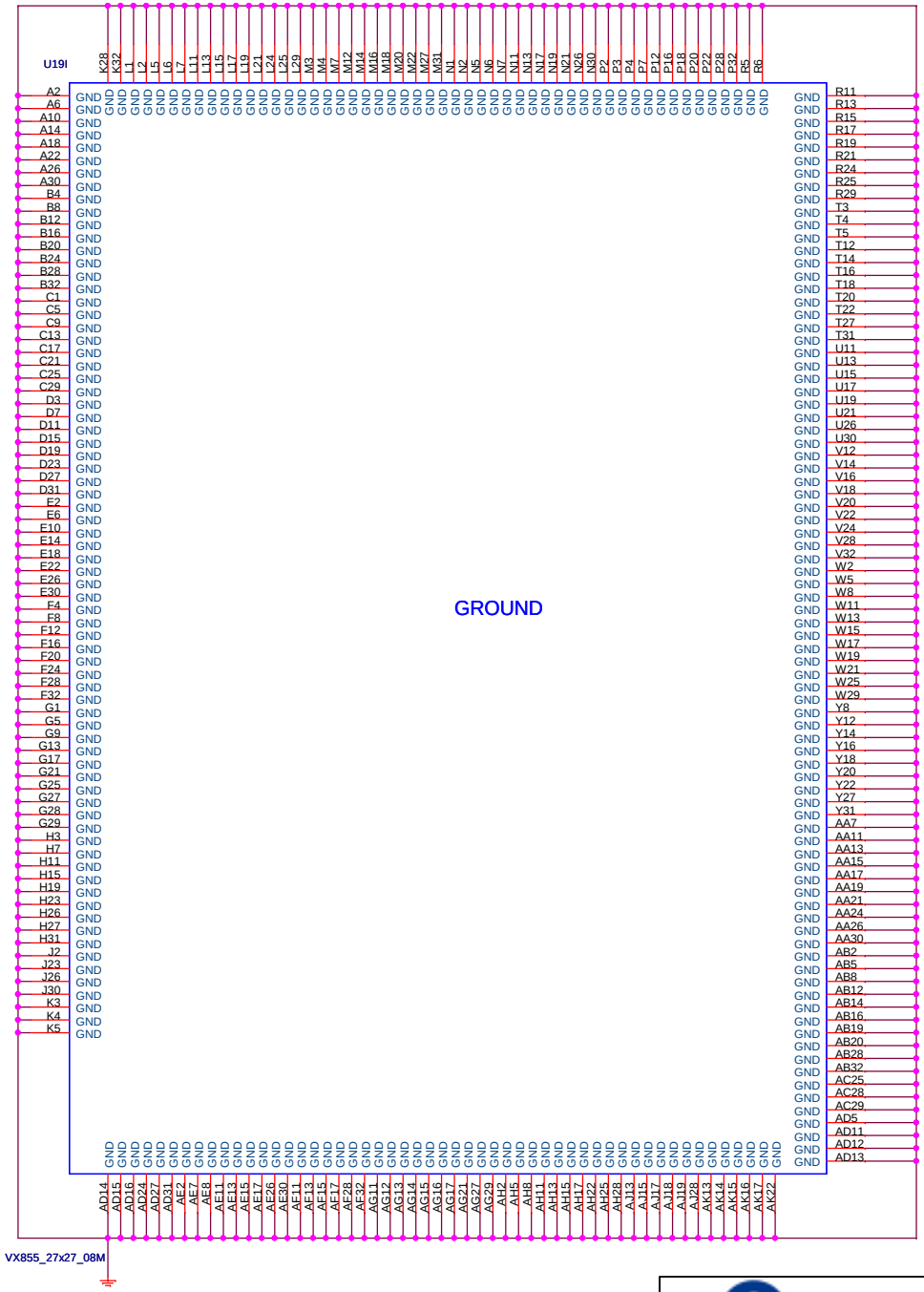

Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number: VX855(U) POWER&GND	Rev: 3A
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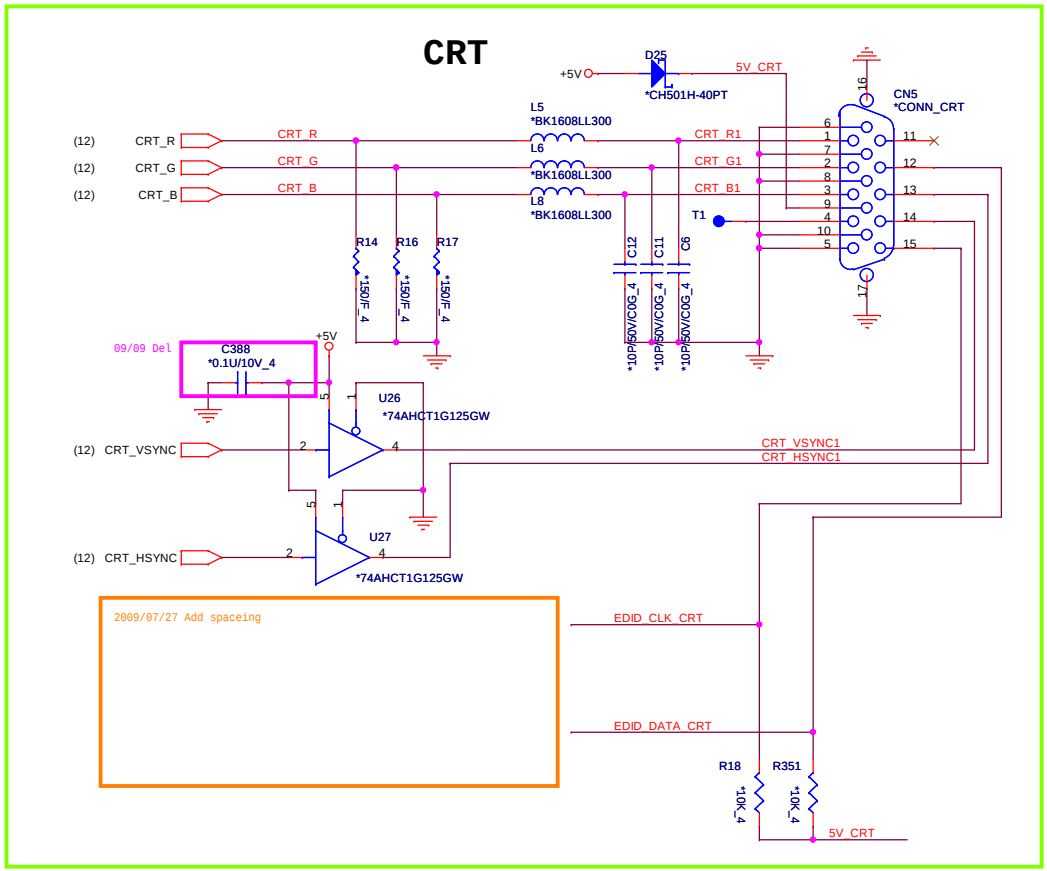
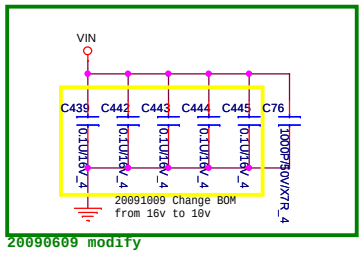
CRT



EMI



20090609 modify

Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number: CRT	Rev: 3A
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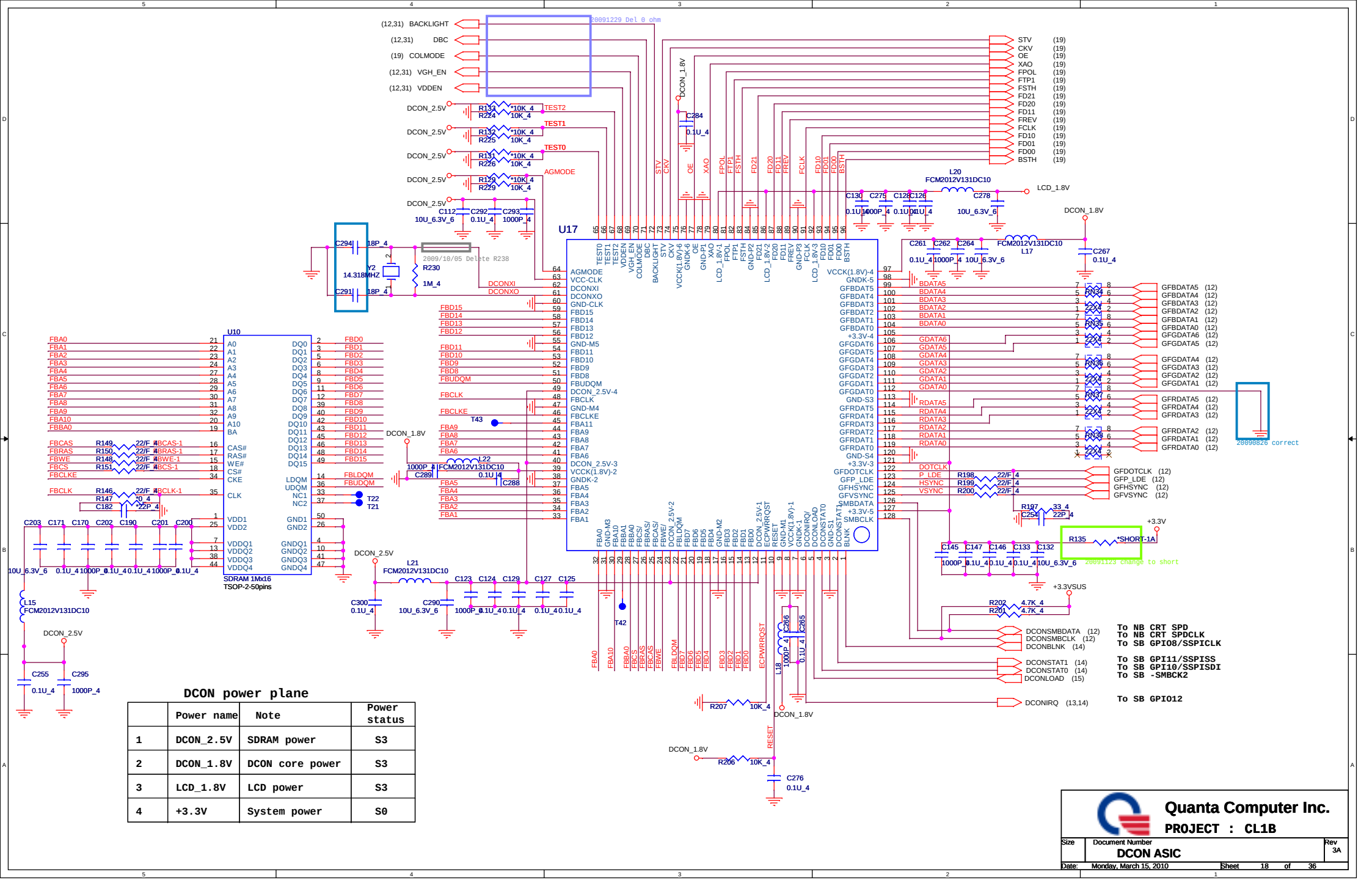

DCON power plane

	Power name	Note	Power status
1	DCON_2.5V	SDRAM power	S3
2	DCON_1.8V	DCON core power	S3
3	LCD_1.8V	LCD power	S3
4	+3.3V	System power	S0

Quanta Computer Inc.

PROJECT : CL1B

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	DCON ASIC	3A

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LCD_1.8V
CN7
CONN-LCD-55P
GND-1
VGH-1
VGL-1
VDD
STV
CKV
OE
XAO
VCOM-1
FPOL
FTP1
FSTH
FD21
FD20
FD11
FREV
FCLK
FD10
FD01
FD00
VDDD-1
VSSD-1
GMA1-1
GMA3-1
GMA5-1
GMA6-1
GMA8-1
GMA10-1
VSSA-1
VDDA-1
VCOM-2
BPOL
BTP1
BSTH
BD21
BD20
BD11
BREV
BCLK
BD10
BD01
BD00
VDDD-2
VSSD-2
GMA1-2
GMA3-2
GMA5-2
GMA6-2
GMA8-2
GMA10-2
VSSA-2
VDDA-2
VGL
VCOM-3
VCOM-4
GND-3
GND-2
LCD_AVDD
9.6V
3VPCU
FP_FCLK
L46
HK1005 33NJ-T
C354
18P_4
20091217 EMI request to add RC filter
CONN_LED-4P
CN3
LEDPWR
LED1
LED2
LED3
VCOM-R: 2.05V
VCOM-T: 2.2V
COLMODE
Q17
*2N7002W-7-F
Q19
2N7002W-7-F
U18
LMV321M5
VCOM-TR
VGH
VGL
VCOM
Quanta Computer Inc.
PROJECT : CL1B
LCD CONNECTOR
Size
Document Number
Rev
3A
Date: Monday, March 15, 2010
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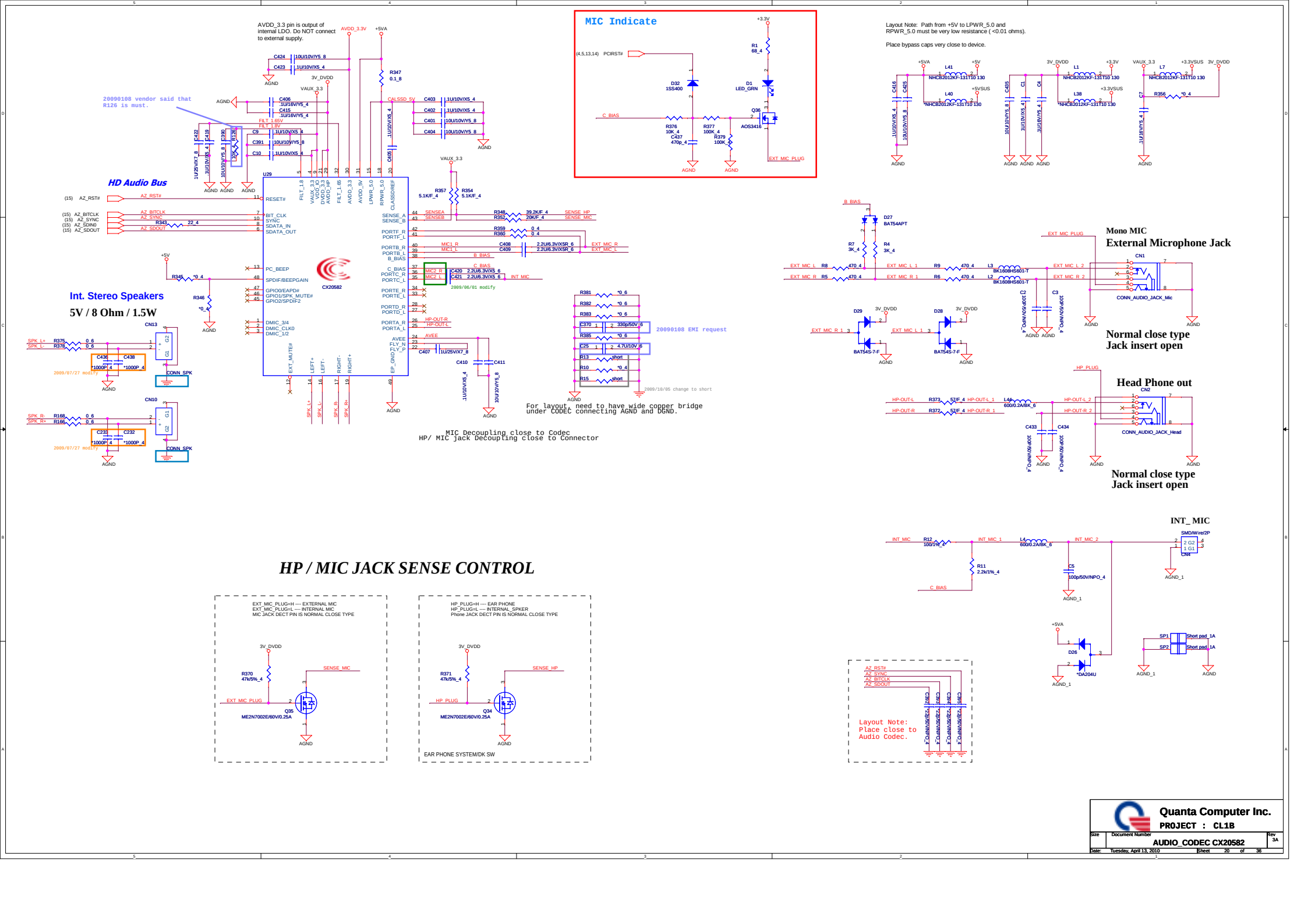
QUANTA CONFIDENTIAL


MIC Indicate
AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.
20090108 vendor said that R126 is must.
HD Audio Bus
Int. Stereo Speakers
5V / 8 Ohm / 1.5W
CX20582
2009/06/01 modify
20090108 EMI request
2009/10/05 change to short
For layout , need to have wide copper bridge under CODEC connecting AGND and DGND.
MIC Decoupling close to Codec
HP/ MIC jack Decoupling close to Connector
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).
Place bypass caps very close to device.
Mono MIC
External Microphone Jack
Normal close type
Jack insert open
Head Phone out
Normal close type
Jack insert open
INT_ MIC
HP / MIC JACK SENSE CONTROL
EXT_MIC_PLUG=H ---- EXTERNAL MIC
EXT_MIC_PLUG=L ---- INTERNAL MIC
MIC JACK DECT PIN IS NORMAL CLOSE TYPE
HP_PLUG=H ---- EAR PHONE
HP_PLUG=L ---- INTERNAL_SPKER
Phone JACK DECT PIN IS NORMAL CLOSE TYPE
EAR PHONE SYSTEM/DK SW
Layout Note:
Place close to
Audio Codec.
Quanta Computer Inc.
PROJECT : CL1B
AUDIO_CODEC CX20582
Rev 3A
Tuesday, April 13, 2010
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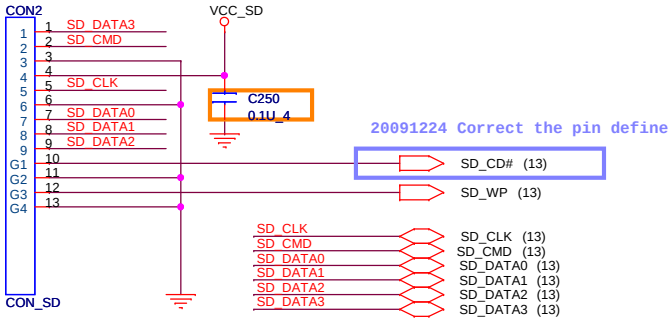
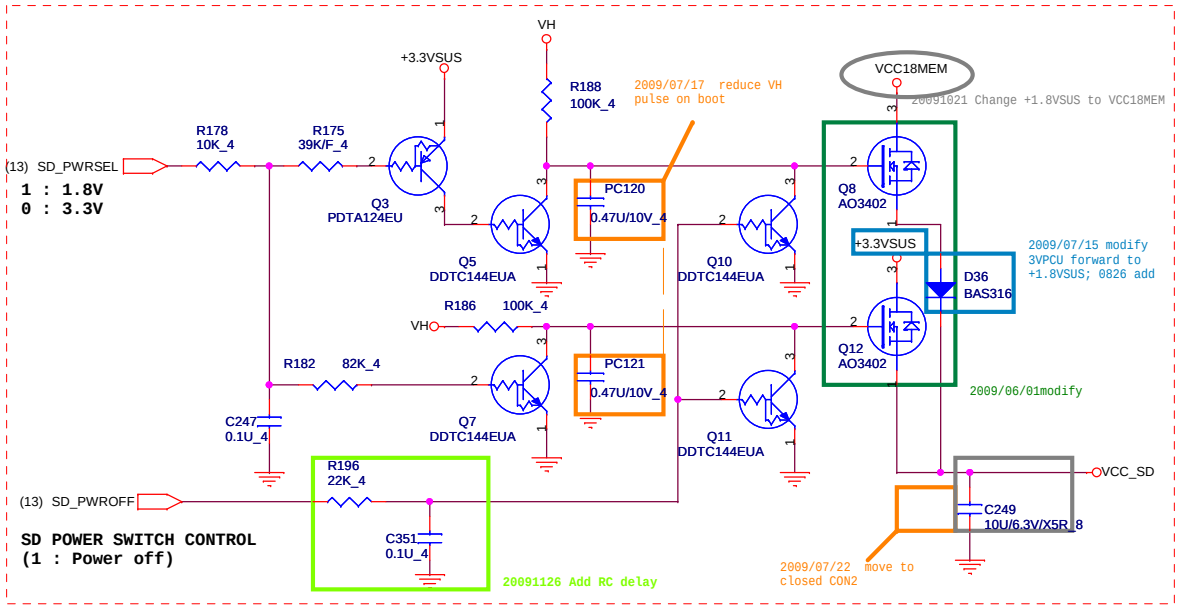
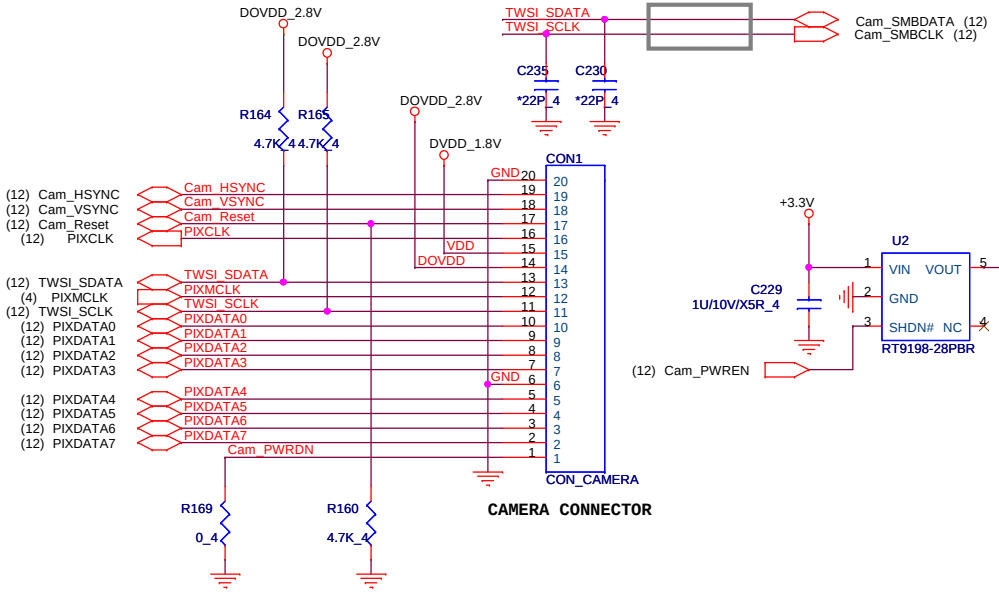


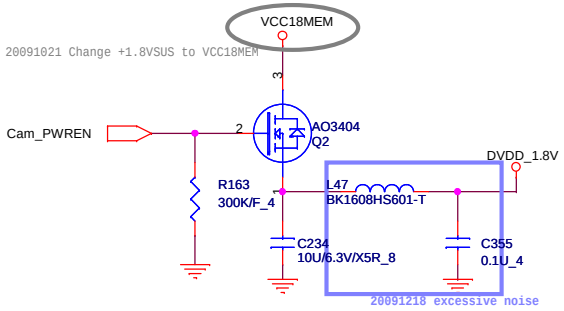
SD Write Protect Detection
(0 : Write Enable, 1 : Write Protect)



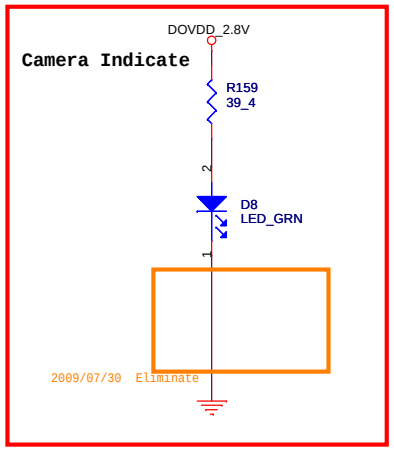
SD POWER SWITCH CONTROL
(1 : Power off)



CAMERA CONNECTOR



Camera POWER SWITCH CONTROL
(1 : Power On)



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Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number	Rev
	NAND FLASH/SD/CAMERA	3A
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Quanta Computer Inc.

PROJECT : CL1B

Size	Document Number	Rev
	NAND FLASH	3A

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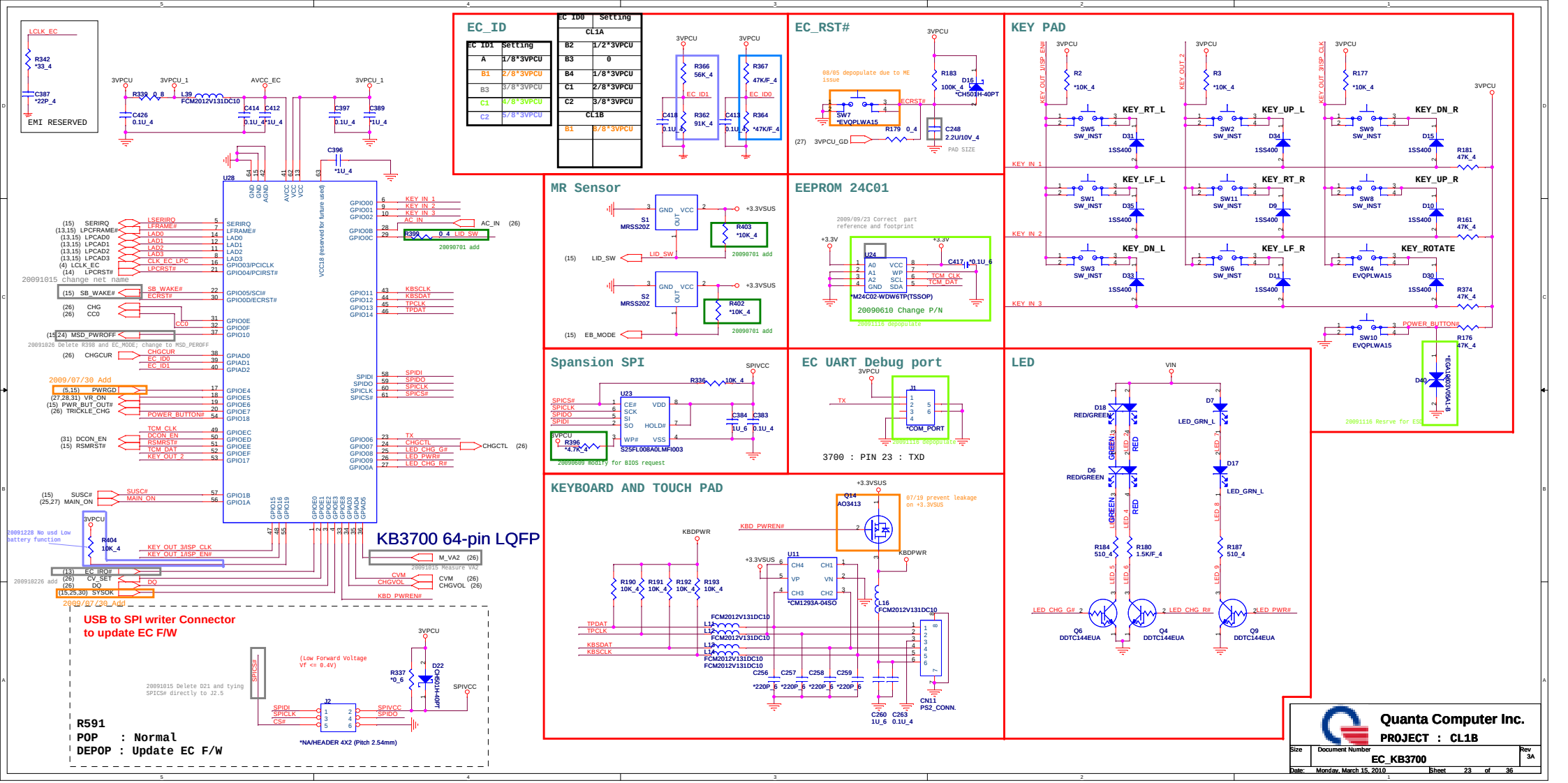
EC_ID
EC_RST#
KEY PAD
MR Sensor
EEPROM 24C01
Spansion SPI
EC UART Debug port
LED
KEYBOARD AND TOUCH PAD
KB3700 64-pin LQFP
USB to SPI writer Connector
to update EC F/W
R591
POP : Normal
DEPOP : Update EC F/W
3700 : PIN 23 : TXD
Quanta Computer Inc.
PROJECT : CL1B
EC_KB3700
Monday, March 15, 2010

GPIO[2] boot-up configuration:
0: JTAG mode enabled (pulled low by 100kohms)
1 and floating: JTAG mode disabled (Default)

[ANT_SEL_N, TR3n] boot-up configuration:
00: General SPI (pulled-low by 100kohms)
11: SDIO (floating is ok)

GPIO[4]:
WLAN MAC wake-up input/interrupt input

ECSn boot-up configuration:
0: Boot up from SPI EEPROM (pulled-low by 100kohms)
1 & floating: Boot up from host interface (Default)

ANT_SEL_N R326 *100K_4
TR3n R324 *100K_4
ECSn R323 *100K_4
WL_GPIO2 R338 *100K_4

Only for SDIO & USB device

20091015 Correct all WLAN schematic

CN19

T90	1	GPIO[4]	2 +3.3V
T91	3	BT_PRIORITY	4 GND
T92	5	WL_ACTIVE	6 1.8V/NC
T93	7	BT_STATE	8 TRSTn
	9	GND	10 TMS_CPU
	11	NC	12 TCK
	13	NC	14 TDO
	15	GND	16 TDI

KEY

(13) SDDA_CD#	17	SD_CD (SD Card Detection)	18 GND
	19	GND	20 PDn
(13) SDDA_CLK	21	SD_CLK/SPI_CLK	22 RESETn
	23	GND	24 3.3V
(13) SDDA_CMD	25	SD_CMD/SPI_SDI	26 GND
(13) SDDA_D0	27	SD_DAT[0]/SPI_SCSn	28 1.8V/NC
(13) SDDA_D1	29	SD_DAT[1]/SPI_SDO	30 NC
(13) SDDA_D2	31	SD_DAT[2]/SPI_SINTn	32 NC
(13) SDDA_D3	33	SD_DAT[3]	34 GND
	35	GND	36 USB_D-
	37	GND	38 USB_D+
	39	3.3V	40 GND
	41	3.3V	42 NC
	43	GND	44 GPIO[1] (LED_WLAN#)
T89 WL_GPIO2	45	GPIO[2]	46 NC
T94 ECSn	47	ECSn	48 SLEEP_CLK
T96 TR3n	49	TR3n	50 GND
T97 ANT_SEL_N	51	ANT_SEL_N	52 3.3V

IC SOCKET MINI PCIE EXP 52P(P0.8,H5.0)
20-25096-00

WLAN_3.3V place at CN19.2
VA18
C455 0.1U/10V_4
C456 0.1U/10V_4
TRSTn T17
TMS_CPU T47
TCK T48
TDO T80
TDI T82
PR156 *100K_4
PR48 10K_4
20091125 Prevent the leakage of WLAN_3.3V
D41 1SS400
WL_RESET# (15)
PDn
C454 0.1U/10V_4 place at CN19.24
C458 0.1U/10V_4 place at CN19.28
WL_USBP5- (15)
WL_USBP5+ (15)
LED_WLAN#
T95
C238 0.1U/10V_4 place at CN19.52
C385 0.1U/10V_4 place at CN19.39

20091021 Change +1.8VSUS to VCC18MEM
VCC18MEM
Q37 AO3420
L45 NHCB2012KF-131T10 130
C453 10U/6.3V/X5_8
R389 47K_4
C368 *0.1U
20091230 for WLAN power sequence

MICRO_SD_3.3V
CON3
(13) MSD_D2
(13) MSD_D3
(13) MSD_CMD
(13) MSD_CLK
(13) MSD_D0
(13) MSD_D1
DAT2
CD/ DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
C379 0.1U_4
CONN MICRO-SD 8P 1R FR(P1.1,H1.97)
20091009 modify and place at CON3.4.

+3.3VSUS
VH
R395 100K_4
AO3404 Q27
0: power on
1: power off
(15,23) MSD_PWROFF
Q28 CHDTC144EUPT
PC122 0.1U/10V_4
MICRO_SD_3.3V
C399 10U/6.3V/X5R_8
20091009 modify and place at CON3.4.

+3.3VSUS
VH
R388 100K_4
20091231 chnge to 0.47ufK to prevent the giltch of WLAN_3.3V
WLAN_PW
AO3404 Q29
1: power off
0: power on
(13) WLAN_EN
R380 47K_4
Q38 CHDTC144EUPT
C331 0.1U
20091125 for WLAN glitch when resuming
C446 0.47U/10V_4
20091218 delete R387 due to no enough spaceng
C452 10U/6.3V/X5_8
C457 *2200P
WLAN_3.3V

VIN
D2 LED_GREEN
D3 LED_GREEN
D24 LED_GREEN
WLAN LED
D23 LED_GREEN
HDD LED
LED 10
LED 13
LED 11
LED 14
LED 12
LED 15
R365 510_4
R344 510_4
+3.3V
(13,14) HDD_LED#/GPIO11

20091229 To prevent the leakage of WLAN_3.3V, change +3.3V to WLAN_3.3V
WLAN_3.3V
LED_WLAN#
D38 1SS400
Q40 PDTA124EU
Q33 DDTC144EUA
Q32 PDTA124EU
Q30 DDTC144EUA

Future Hacking

+5VSUS
R392 *0_8
R393 *0_8
HA_USBP4+ (15)
HA_USBP4- (15)
20090730 Add

Quanta Computer Inc.			
PROJECT : CL1B			
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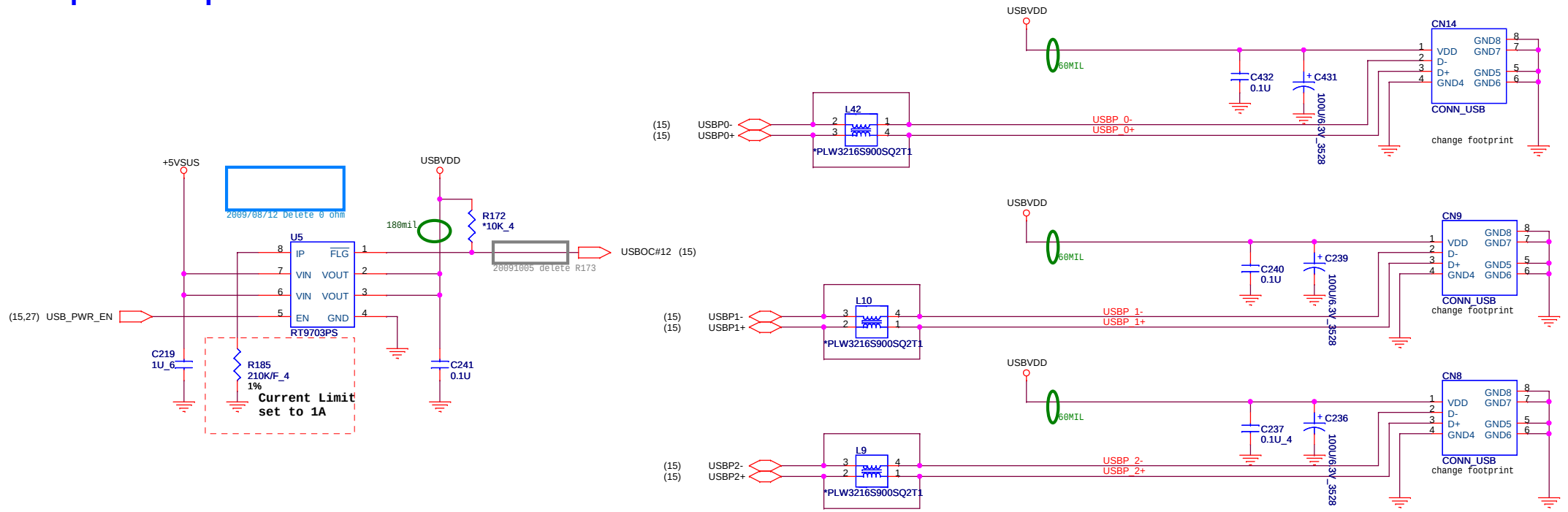
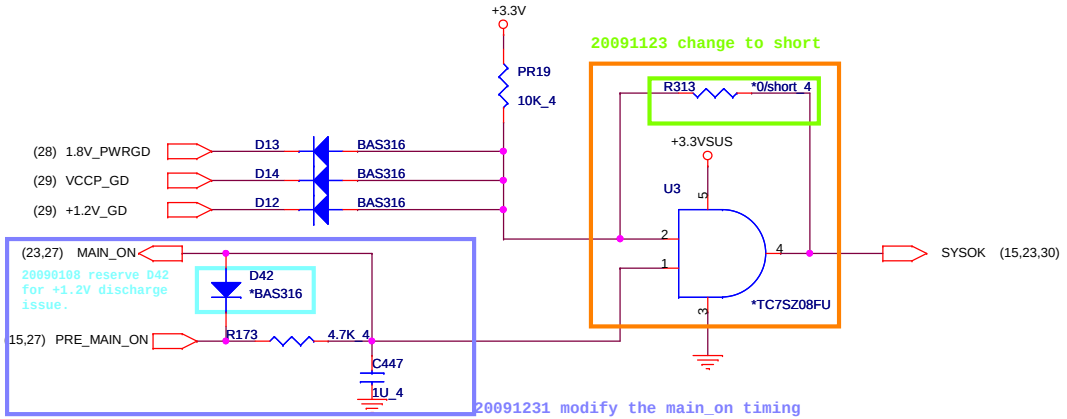
USB power / port



Reset circuit



Quanta Computer Inc.		
PROJECT : CL1B		
Size	Document Number	Rev
	USB	3A
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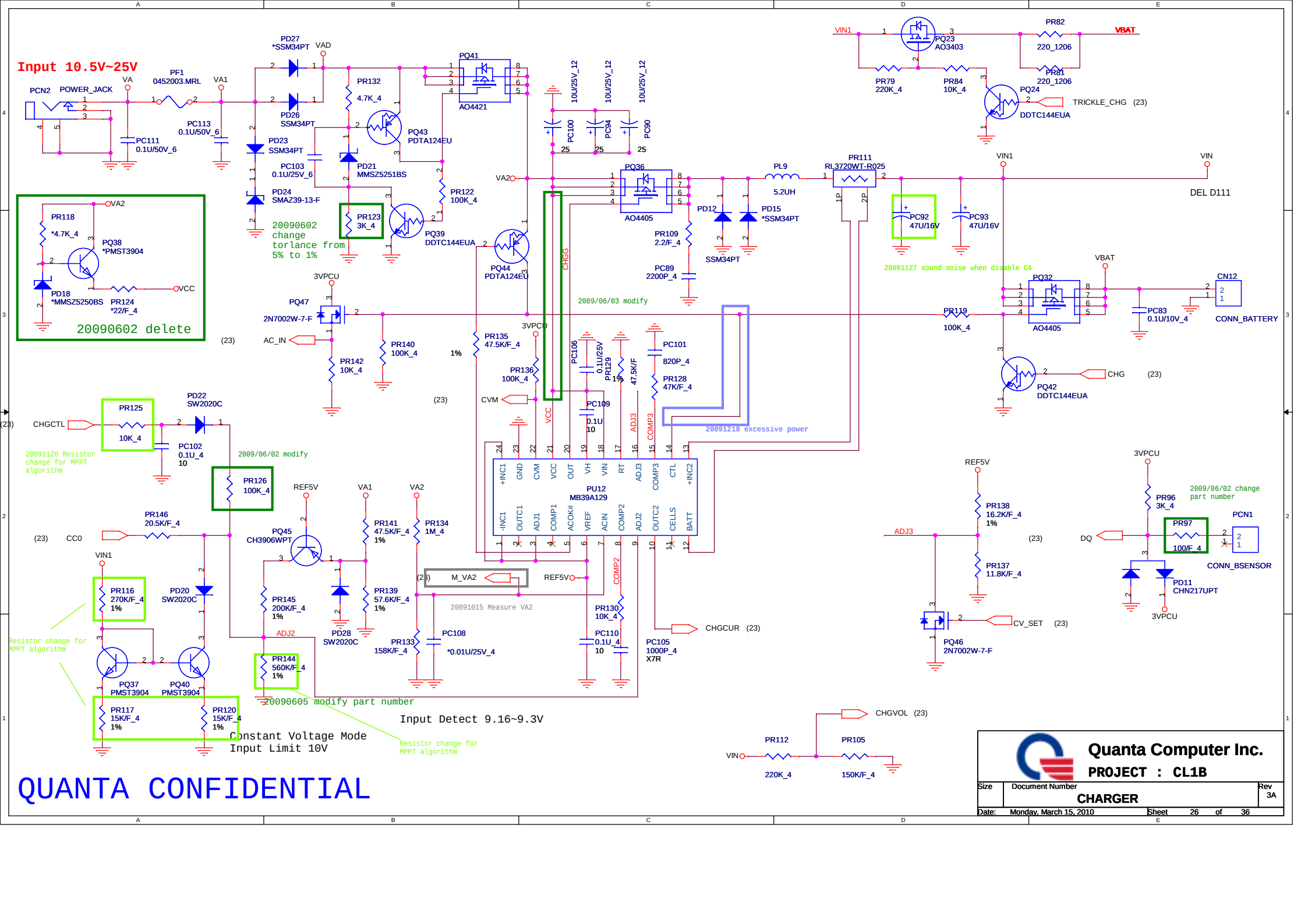
Input 10.5V~25V
PCN2 POWER_JACK
PF1 0452003.MRL
PC111 0.1U/50V_6
PC113 0.1U/50V_6
PD27 *SSM34PT
PD26 SSM34PT
PD23 SSM34PT
PD24 SMAZ39-13-F
PC103 0.1U/25V_6
PD21 MMSZ5251BS
PR132 4.7K_4
PQ43 PDTA124EU
PQ41 AO4421
PR122 100K_4
PR123 3K_4
PQ39 DDTC144EUA
20090602 change torlance from 5% to 1%
PR118 *4.7K_4
PQ38 *PMST3904
PD18 *MMSZ5250BS
PR124 *22/F_4
20090602 delete
PC100 10U/25V_12
PC94 10U/25V_12
PC90 10U/25V_12
PQ36 AO4405
PD12
PD15 *SSM34PT
PL9 5.2UH
PR109 2.2/F_4
PC89 2200P_4
PR111 RL3720WT-R025
PC92 47U/16V
PC93 47U/16V
20091127 sound noise when disable C4
PQ32 AO4405
PC83 0.1U/10V_4
CN12 CONN_BATTERY
PR119 100K_4
PQ42 DDTC144EUA
CHG (23)
PQ47 2N7002W-7-F
AC_IN (23)
PR140 100K_4
PR142 10K_4
2009/06/03 modify
PR135 47.5K/F_4
PR136 100K_4
PC106 0.1U/25V
PR129 47.5K/F_4 1%
PC101 820P_4
PR128 47K/F_4
20091218 excessive power
CVM (23)
PC109 0.1U 10
PU12 MB39A129
+INC1 GND CVM VCC OUT VH VIN RT ADJ3 COMP3 CTL +INC2
-INC1 OUTC1 ADJ1 COMP1 ACOK# VREF ACIN COMP2 ADJ2 OUTC2 CELLS BATT
PR125 10K_4
PD22 SW2020C
PC102 0.1U_4 10
CHGCTL (23)
20091120 Resistor change for MPPT algorithm
2009/06/02 modify
PR126 100K_4
PR146 20.5K/F_4
CC0 (23)
VIN1
PR116 270K/F_4 1%
PD20 SW2020C
PQ37 PMST3904
PQ40 PMST3904
PR117 15K/F_4 1%
PR120 15K/F_4 1%
Resistor change for MPPT algorithm
Constant Voltage Mode
Input Limit 10V
PQ45 CH3906WPT
PR145 200K/F_4 1%
PD28 SW2020C
PR141 47.5K/F_4 1%
PR139 57.6K/F_4 1%
PR134 1M_4
PR133 158K/F_4
PC108 *0.01U/25V_4
M_VA2 (23)
20091015 Measure VA2
PR130 10K_4
PC110 0.1U_4 10
PC105 1000P_4 X7R
CHGCUR (23)
PR144 560K/F_4 1%
20090605 modify part number
Input Detect 9.16~9.3V
Resistor change for MPPT algorithm
PR138 16.2K/F_4 1%
PR137 11.8K/F_4
ADJ3
CV_SET (23)
PQ46 2N7002W-7-F
PR96 3K_4
PR97 100/F_4
2009/06/02 change part number
PCN1 CONN_BSENSOR
PD11 CHN217UPT
DQ
PR112 220K_4
PR105 150K/F_4
CHGVOL (23)
VIN1
PR82 220_1206
PR81 220_1206
PR79 220K_4
PR84 10K_4
PQ23 AO3403
PQ24 DDTC144EUA
TRICKLE_CHG (23)
VBAT
DEL D111
QUANTA CONFIDENTIAL
Quanta Computer Inc.
PROJECT : CL1B
Size
Document Number
CHARGER
Rev 3A
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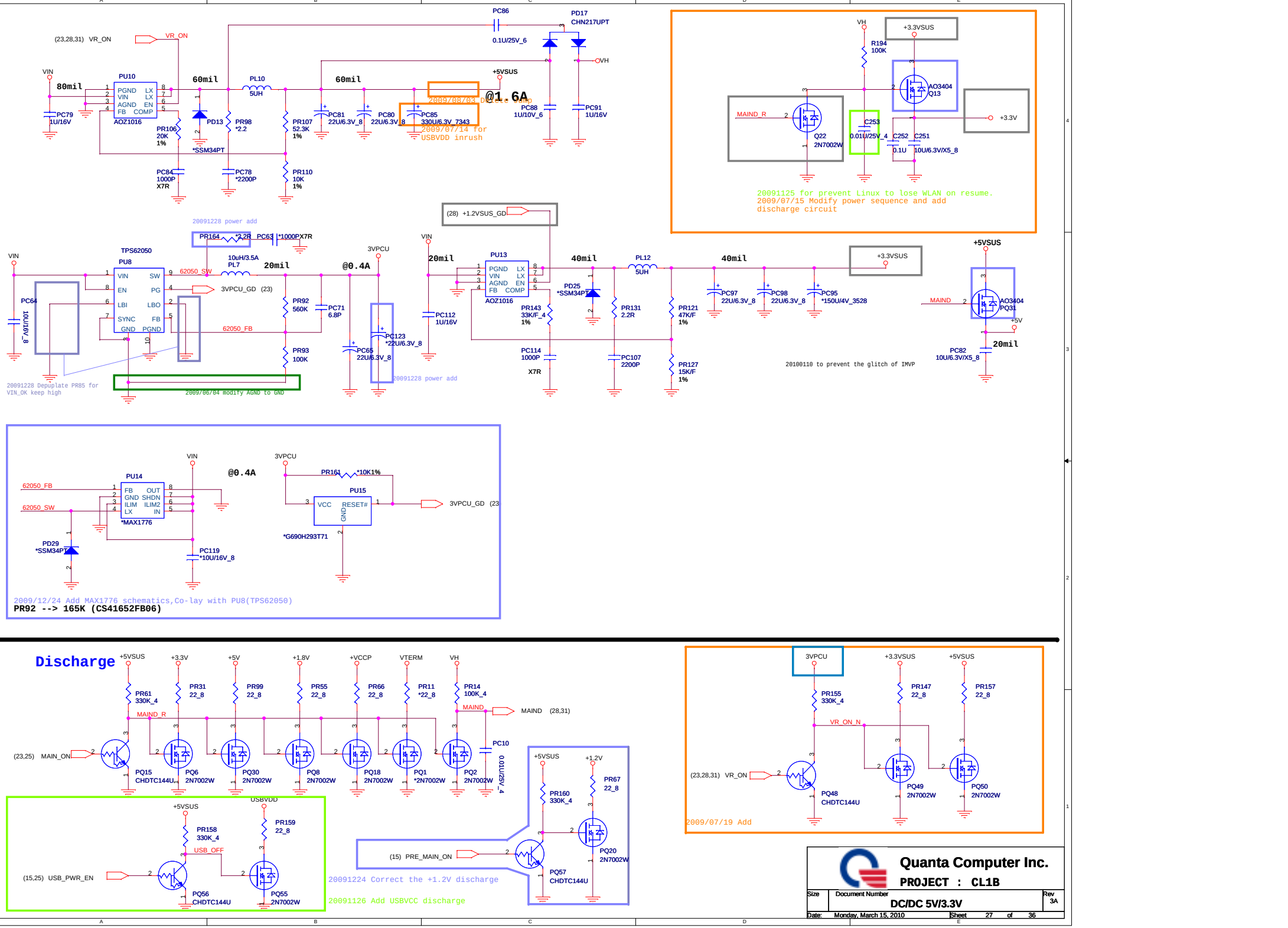
(23,28,31) VR_ON
VR_ON
VIN
80mil
PU10
PGND LX
VIN LX
AGND EN
FB COMP
AOZ1016
PC79
1U/16V
PR106
20K
1%
*SSM34PT
PD13
PR98
*2.2
60mil
PL10
5UH
PR107
52.3K
1%
PC84
1000P
X7R
PC78
*2200P
PR110
10K
1%
60mil
PC81
22U/6.3V_8
PC80
22U/6.3V_8
PC85
330U/6.3V_7343
2009/07/14 for
USBVDD inrush
PC86
0.1U/25V_6
PD17
CHN217UPT
VH
+5VSUS
@1.6A
PC88
1U/10V_6
PC91
1U/16V
20091228 power add
PR164
*2.2R
PC63
*1000PX7R
TPS62050
PU8
VIN SW
EN PG
LBI LBO
SYNC FB
GND PGND
10uH/3.5A
PL7
62050_SW
20mil
3VPCU_GD (23)
62050_FB
PR92
560K
PC71
6.8P
PR93
100K
PC64
10U/16V_8
@0.4A
3VPCU
PC123
*22U/6.3V_8
PC65
22U/6.3V_8
20091228 Depuplate PR85 for
VIN_OK keep high
2009/08/04 modify AGND to GND
20091228 power add
(28) +1.2VSUS_GD
VIN
20mil
PU13
PGND LX
VIN LX
AGND EN
FB COMP
AOZ1016
PC112
1U/16V
40mil
PD25
*SSM34PT
PR143
33K/F_4
1%
PC114
1000P
X7R
PL12
5UH
PR131
2.2R
PC107
2200P
PR127
15K/F
1%
40mil
PR121
47K/F
1%
PC97
22U/6.3V_8
PC98
22U/6.3V_8
PC95
*150U/4V_3528
+3.3VSUS
20100110 to prevent the glitch of IMVP
+5VSUS
MAIND
AO3404
PQ31
+5V
20mil
PC82
10U/6.3V/X5_8
VH
+3.3VSUS
R194
100K
AO3404
Q13
MAIND_R
Q22
2N7002W
C253
0.01U/25V_4
C252
0.1U
C251
10U/6.3V/X5_8
+3.3V
20091125 for prevent Linux to lose WLAN on resume.
2009/07/15 Modify power sequence and add
discharge circuit
VIN
PU14
FB OUT
GND SHDN
ILIM ILIM2
LX IN
*MAX1776
62050_FB
62050_SW
@0.4A
PD29
*SSM34PT
PC119
*10U/16V_8
3VPCU
PR161
*10K1%
PU15
VCC RESET#
GND
*G690H293T71
3VPCU_GD (23
2009/12/24 Add MAX1776 schematics,Co-lay with PU8(TPS62050)
PR92 --> 165K (CS41652FB06)
Discharge
+5VSUS
+3.3V
+5V
+1.8V
+VCCP
VTERM
VH
PR61
330K_4
PR31
22_8
PR99
22_8
PR55
22_8
PR66
22_8
PR11
*22_8
PR14
100K_4
MAIND_R
MAIND
MAIND (28,31)
PC10
0.01U/25V_4
(23,25) MAIN_ON
PQ15
CHDTC144U
PQ6
2N7002W
PQ30
2N7002W
PQ8
2N7002W
PQ18
2N7002W
PQ1
*2N7002W
PQ2
2N7002W
USBVDD
PR158
330K_4
PR159
22_8
USB_OFF
(15,25) USB_PWR_EN
PQ56
CHDTC144U
PQ55
2N7002W
20091126 Add USBVCC discharge
+5VSUS
+1.2V
PR160
330K_4
PR67
22_8
(15) PRE_MAIN_ON
PQ57
CHDTC144U
PQ20
2N7002W
20091224 Correct the +1.2V discharge
3VPCU
+3.3VSUS
+5VSUS
PR155
330K_4
PR147
22_8
PR157
22_8
VR_ON_N
(23,28,31) VR_ON
PQ48
CHDTC144U
PQ49
2N7002W
PQ50
2N7002W
2009/07/19 Add
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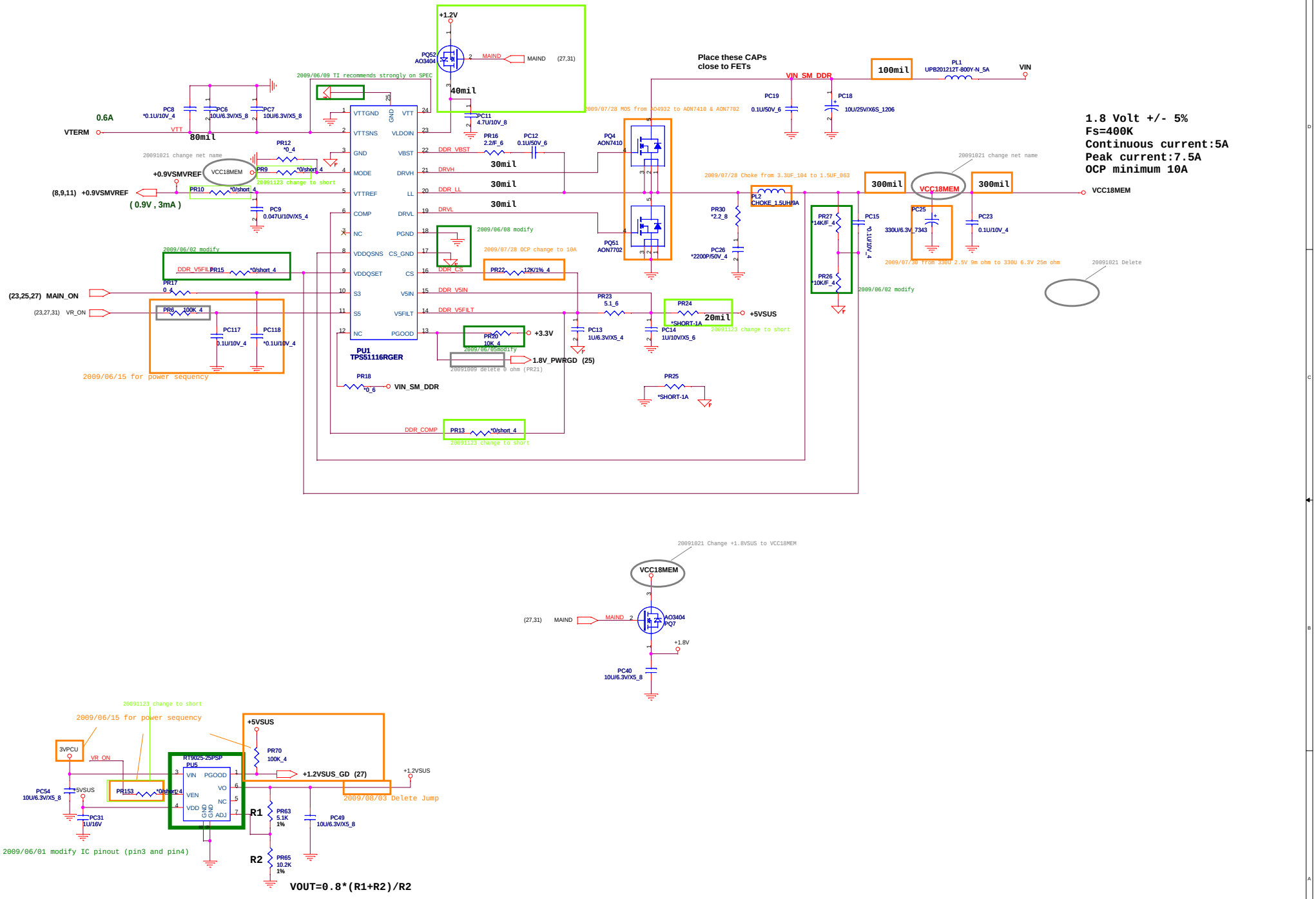

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	DDRII/+0.9V(TPS51116)	3A
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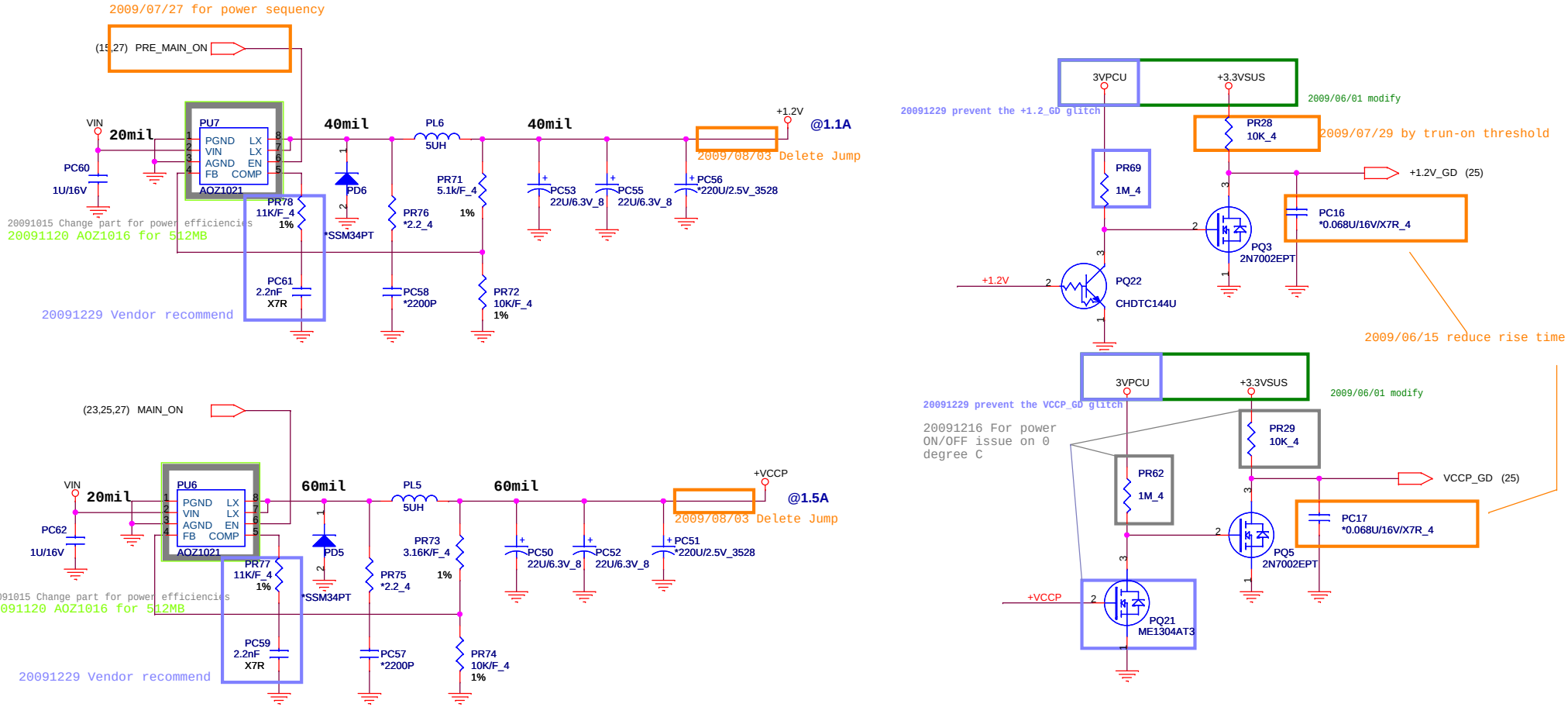

Vo=0.8 x (1+(R2/R3))

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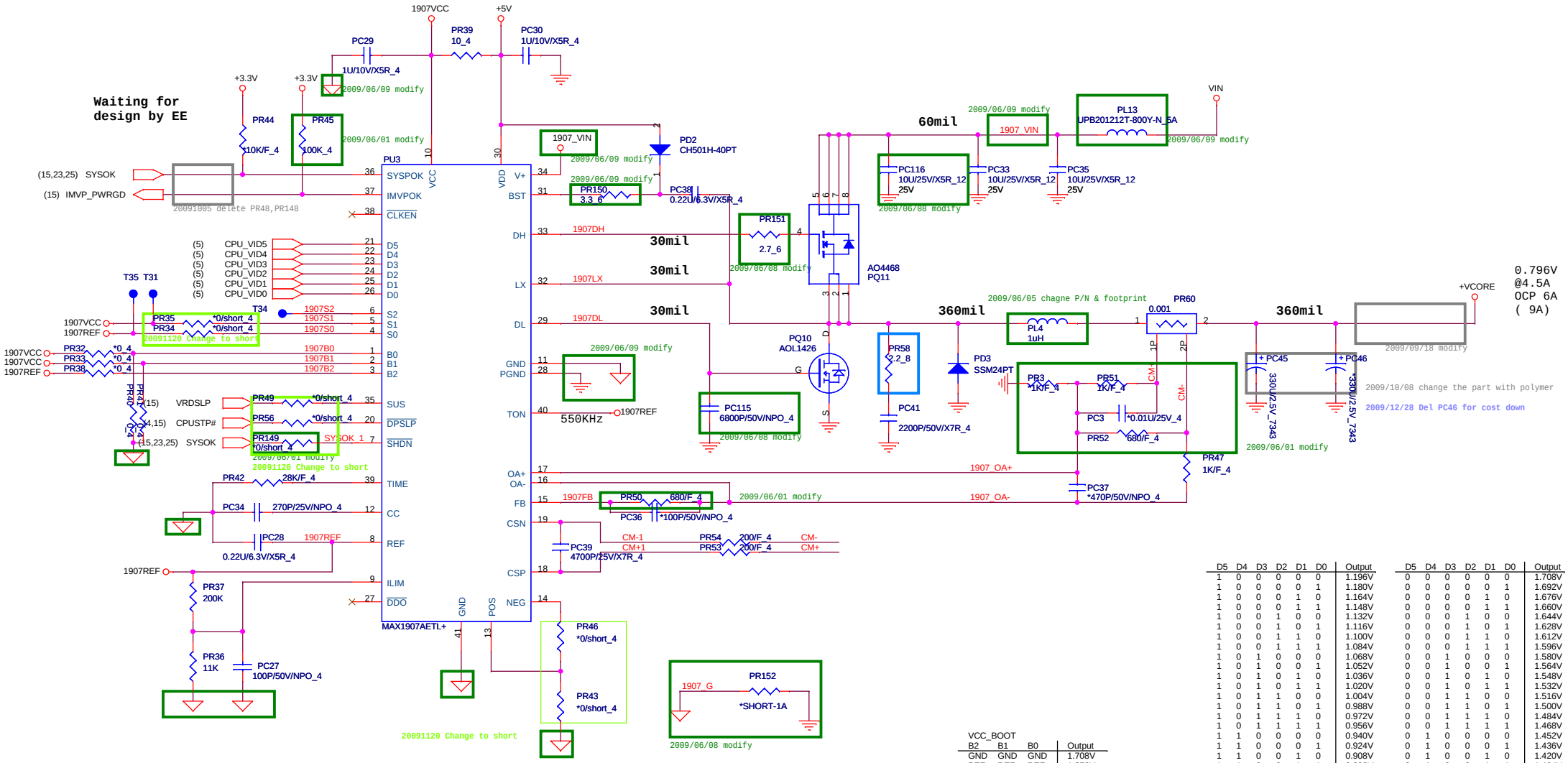
CPU CORE(MAX1907)



VCC_BOOT			
B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
REF	VCC	VCC	1.212V
OPEN	GND	GND	1.196V

SUSPEND MODE (SUS=HIGH)			
S2	S1	S0	Output
OPEN	OPEN	OPEN	0.780V
OPEN	VCC	REF	0.732V (0.724V)

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V
1	0	0	0	0	1	1.180V
1	0	0	0	1	0	1.164V
1	0	0	0	1	1	1.148V
1	0	0	1	0	0	1.132V
1	0	0	1	0	1	1.116V
1	0	0	1	1	0	1.100V
1	0	0	1	1	1	1.084V
1	0	1	0	0	0	1.068V
1	0	1	0	0	1	1.052V
1	0	1	0	1	0	1.036V
1	0	1	0	1	1	1.020V
1	0	1	1	0	0	1.004V
1	0	1	1	0	1	0.988V
1	0	1	1	1	0	0.972V
1	0	1	1	1	1	0.956V
1	1	0	0	0	0	0.940V
1	1	0	0	0	1	0.924V
1	1	0	0	1	0	0.908V
1	1	0	0	1	1	0.892V
1	1	0	1	0	0	0.876V
1	1	0	1	0	1	0.860V
1	1	0	1	1	0	0.844V
1	1	0	1	1	1	0.828V
1	1	1	0	0	0	0.812V
1	1	1	0	0	1	0.796V
1	1	1	0	1	0	0.780V
1	1	1	0	1	1	0.764V
1	1	1	1	0	0	0.748V
1	1	1	1	0	1	0.732V
1	1	1	1	1	0	0.716V
1	1	1	1	1	1	0.700V

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.708V
0	0	0	0	0	1	1.692V
0	0	0	0	1	0	1.676V
0	0	0	0	1	1	1.660V
0	0	0	1	0	0	1.644V
0	0	0	1	0	1	1.628V
0	0	0	1	1	0	1.612V
0	0	0	1	1	1	1.596V
0	0	1	0	0	0	1.580V
0	0	1	0	0	1	1.564V
0	0	1	0	1	0	1.548V
0	0	1	0	1	1	1.532V
0	0	1	1	0	0	1.516V
0	0	1	1	0	1	1.500V
0	0	1	1	1	0	1.484V
0	0	1	1	1	1	1.468V
0	1	0	0	0	0	1.452V
0	1	0	0	0	1	1.436V
0	1	0	0	1	0	1.420V
0	1	0	0	1	1	1.404V
0	1	0	1	0	0	1.388V
0	1	0	1	0	1	1.372V
0	1	0	1	1	0	1.356V
0	1	0	1	1	1	1.340V
0	1	1	0	0	0	1.324V
0	1	1	0	0	1	1.308V
0	1	1	0	1	0	1.292V
0	1	1	0	1	1	1.276V
0	1	1	1	0	0	1.260V
0	1	1	1	0	1	1.244V
0	1	1	1	1	0	1.228V
0	1	1	1	1	1	1.212V

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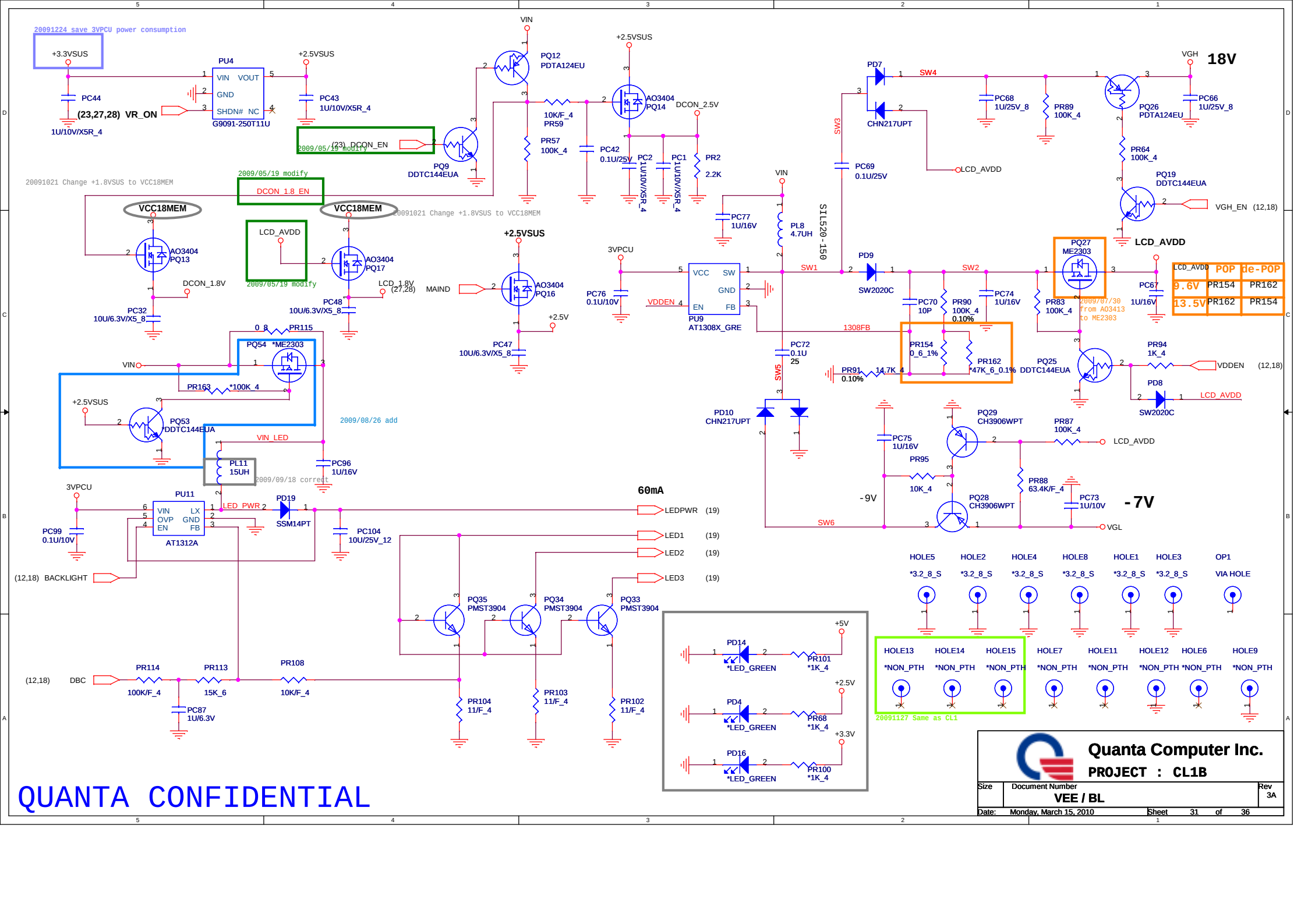
20091224 save 3VPCU power consumption
+3.3VSUS
PU4
VIN VOUT
GND
SHDN# NC
G9091-250T11U
+2.5VSUS
PC44
1U/10V/X5R_4
(23,27,28) VR_ON
PC43
1U/10V/X5R_4
(23) DCON_EN
2009/05/19 modify
PQ9
DDTC144EUA
VIN
PQ12
PDTA124EU
10K/F_4
PR59
PR57
100K_4
AO3404
PQ14
DCON_2.5V
PC42
0.1U/25V
PC2
1U/10V/X5R_4
PC1
1U/10V/X5R_4
PR2
2.2K
20091021 Change +1.8VSUS to VCC18MEM
2009/05/19 modify
DCON_1.8_EN
VCC18MEM
AO3404
PQ13
DCON_1.8V
PC32
10U/6.3V/X5_8
LCD_AVDD
2009/05/19 modify
AO3404
PQ17
LCD_1.8V
(27,28)
PC48
10U/6.3V/X5_8
20091021 Change +1.8VSUS to VCC18MEM
+2.5VSUS
AO3404
PQ16
MAIND
+2.5V
PC47
10U/6.3V/X5_8
0_8
PR115
PQ54 *ME2303
VIN
PR163
*100K_4
+2.5VSUS
PQ53
*DDTC144EUA
2009/08/26 add
VIN_LED
PL11
15UH
2009/09/18 correct
PC96
1U/16V
3VPCU
PU11
VIN LX
OVP GND
EN FB
AT1312A
LED_PWR
PD19
SSM14PT
PC99
0.1U/10V
PC104
10U/25V_12
60mA
LEDPWR (19)
LED1 (19)
LED2 (19)
LED3 (19)
(12,18) BACKLIGHT
PQ35
PMST3904
PQ34
PMST3904
PQ33
PMST3904
(12,18) DBC
PR114
100K/F_4
PR113
15K_6
PR108
10K/F_4
PC87
1U/6.3V
PR104
11/F_4
PR103
11/F_4
PR102
11/F_4
PD14
*LED_GREEN
PR101
*1K_4
+5V
PD4
*LED_GREEN
PR68
*1K_4
+2.5V
PD16
*LED_GREEN
PR100
*1K_4
+3.3V
VIN
PC77
1U/16V
PL8
4.7UH
SI1520-150
3VPCU
PC76
0.1U/10V
VDDEN
PU9
AT1308X_GRE
VCC SW
GND
EN FB
SW1
1308FB
PC72
0.1U
25
SW5
PD10
CHN217UPT
PD7
SW4
CHN217UPT
SW3
PC69
0.1U/25V
LCD_AVDD
PD9
SW2020C
SW2
PC70
10P
PR90
100K_4
0.10%
PC74
1U/16V
PR154
0_6_1%
PR162
*47K_6_0.1%
PR91
14.7K_4
0.10%
SW6
PC75
1U/16V
PR95
10K_4
-9V
PQ29
CH3906WPT
PQ28
CH3906WPT
PR87
100K_4
PR88
63.4K/F_4
PC73
1U/10V
-7V
VGL
VGH
18V
PC68
1U/25V_8
PR89
100K_4
PQ26
PDTA124EU
PC66
1U/25V_8
PR64
100K_4
PQ19
DDTC144EUA
VGH_EN (12,18)
LCD_AVDD
PQ27
ME2303
2009/07/30
from AO3413
to ME2303
PC67
1U/16V
PR83
100K_4
PQ25
DDTC144EUA
PR94
1K_4
VDDEN (12,18)
PD8
SW2020C
LCD_AVDD
LCD_AVDD POP de-POP
9.6V PR154 PR162
13.5V PR162 PR154
HOLE5 *3.2_8_S
HOLE2 *3.2_8_S
HOLE4 *3.2_8_S
HOLE8 *3.2_8_S
HOLE1 *3.2_8_S
HOLE3 *3.2_8_S
OP1 VIA HOLE
HOLE13 *NON_PTH
HOLE14 *NON_PTH
HOLE15 *NON_PTH
HOLE7 *NON_PTH
HOLE11 *NON_PTH
HOLE12 *NON_PTH
HOLE6 *NON_PTH
HOLE9 *NON_PTH
20091127 Same as CL1
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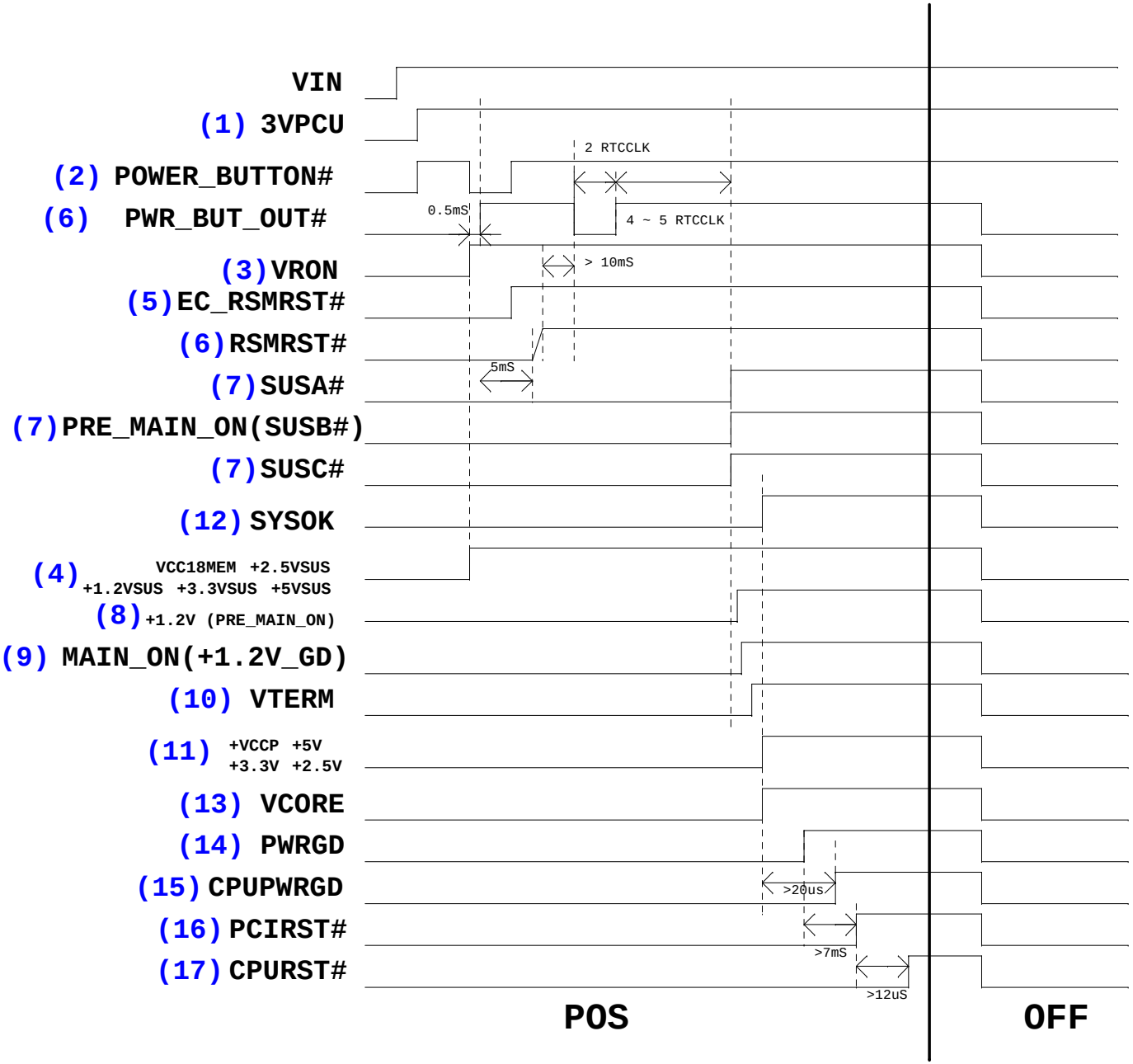

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Schematic modify Item and History :

A1-->A2

1. *DCON POWER* -
   - A. Change PQ9.B pin from DCON_1.8 to DCON_EN
   - B. Change PQ13.G pin from DCON_EN to PQ12.C
   - C. Change PQ17.G pin from VDDEN to LCD_AVDD
2. *SB straping* -
   - A. Change R27, R83, R270, R54, R34, R87, R78 and R82 from 4.7K ohm to 1K ohm.
3. *Design issue* -
   - A.The D pin and S pin of Q8 and Q12 is inverse
   - B.Change C299 part number
   - C.Add test points: U28, pins 1, 4, 17, 29, 36, and 37
   - d.Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L
   - e.RTC issue: VIA recommend to delete R216
4. *Power* -
   - A.1.8VSUS
     - a. Add off-page connector : VR_ON
     - b. Modify PU5 pinout.
     - C. For +1.8VUSU sense: stuff PR15 ; don't stuff PR27 and PR26
     - d. For +1.8VUSU OCP : modify PR22 from 4.99K to 6.2K, OCP from 3A to 3.5A
     - e. modify PU1 pin11 net name to VR_ON
   - B.+VCORE:
     - a.For SYSOK PULL HIGH: Stuff PR45
     - b.For +VCORE sense: don't stuff PC3 & PR3 ; stuff PR51 & PR52
     - c.For CPU Load line : for meet load line -1mV/A, modify PR52 & PR50 from 1K to 680 ohm
   - C.1.2 and +VCCP:
     - a.Modify power good circuit: change net name from 3.3VSUS to +3.3VSUS
   - D.Charger :
     - a.Delete clamp circuit (PR118,PD18,PQ38,PR124):
       PU12 (MB39A129) can guaranty to 28V
     - b.connect PU12 pin21 to PQ36 pin1,2,3 directly
     - c.change PR126 to 100K
5. *WLAN*-
   - Change WLAN solution from SD card to TM100 module. See page 24

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Schematic modify Item and History :

A2-->B1

2. SDIO

A. SDIO:Micro SD
B. SDIO1: SD Card Reader
C. SDIO2: WLAN module

2. SB straping -

A. Change R58, R170 and R195 pull up power plane on page13

3. Design issue -

A.Modify CPU RST circuit
  a.Add R248 0 ohm
  b.Populate Q18,Q20 R275 to prevent leakage for vendor's recommand.
  c.Del c299 for CPU power good delay time
B.Del SPI ROM of memory
C.Modify DCONLOAD and WLAN_RESET# to U19.AG20 and AF21
D.Modify Serial enable to U19.AJ21
E.Modify THRM# pin of U19 from PROCHOT# to EB_MODE
F.Del EDID_CLK and EDID_DATA of CRT circuit
G.Del R195 within GDATA0 pull low
H.Rerevse C436,C438, C233 and C232 for EMI/ESD
I.Add PC120 and PC121 for VH gilch and add D36 to prevent 3VPU forward to +1.8VSUS
J.Move C250 to close CON2 and modify CAM LED control.
K.Del NAND flash on page 22
L.Add PWRGD net on U28.17 & SYSOK on U28.4 & change M/B ID & Del SW7 on page 23
M. change Q14 from PNP BJT to P-MOS
N. Change WLAN solution from on board to slot and correct WLAN LED behavior on page 24.
O. Add Micro SD on page 24.
P. Correct power good circuit on page 25.

4. Power -

A.Del all jump,but only reserve the jump of +VCCORE and +1.8VSUS.

A.1.8VSUS
  a. Add off-page connector : VR_ON
  b. Modify PU5 pinout.
  d. For +1.8VUSU OCP : modify PR22 from 4.99K to 6.2K, OCP from 3A to 3.5A
B.+VCORE:
  a.For SYSOK PULL HIGH: Stuff PR45
  b.For +VCORE sense: don't stuff PC3 & PR3 ; stuff PR51 & PR52
  c.For CPU Load line : for meet load line -1mV/A, modify PR52 & PR50 from 1K to 680 ohm
D.Charger :

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Schematic modify Item and History :

B2-->B3

1. Power -

A. Change PL11 from 4.7uH to 15uH

B. Delete PJP5

2. Design issue -

A.Correct part refence from 12 to U24

B.Change C299 part number

C.Add test points: U28, pins 1, 4, 17, 29, 36, and 37

d.Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L

e.RTC issue: VIA recommend to delete R216

1. DCON POWER -

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Schematic modify Item and History :

C1-->C2

1. Power -

A. PU6/PU7 (AOZ1021): correct the R/C of comp pin to 11K and 2.2nF

B. Change the PQ21 from CHDTC144U to ME1304AT3 (Vgs<1V)

page 27 C. Correct the +3.3VSUS to 3VPCU on PR69.1 and PR62 for prevent the +1.2V_GD glitch

D. Change the Q13 and PQ31 to AO3404 for power good giltch by +3.3V & 5V sequence issue on PU3

E. Add MAX1776 circuit for TPS62050 L/T time isn't enough.

F. Correct the +1.2V discharge circuit

page 26 G. modify the PU12.14 and connect to PQ44.3 for excessive power

page 25 H. Add R/C delay on PRE_MAIN_ON to conrtol MAIN_ON for S3 issue and reserve the D42 between MAIN_ON and PRE_MAIN_ON 3 quickly +1.2V discharge

page 24 I. Correct the Q37.2 form WL_SW to WLAN_3.3V for WLAN power sequence

J. Change the C446 to 0.47uf for prevent the giltch of WLAN_3.3V

K. Change the Q40.1 from +3.3V to WLAN_3.3V to prevent the leakage of WLAN_3.3V

page 23 L. Pull high on U28.55 for un-usd Low battery function

M. correct the R366 and R362 for EC_ID

page 21 N. SWAP the CON2.10 and CON.11

O.Add L/C on Q2.1 for DVDD_1.8V excessive noise.

page 20 P.For EMI request, change R384 to C370 & R386 to C25

Q.Change C8 to R126 for preventing no sound on speaker when S3/reboot resume.

F. Power team suggest:

1.Reserve PC123, PR164.

2.Short the PU8.2 & PU8.6 to GND for Vin_OK keep high

2. Design issue -

A.Correct part refence from 12 to U24

B.Change C299 part number

C.Add test points: U28, pins 1, 4, 17, 29, 36, and 37

d.Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L

e.RTC issue: VIA recommend to delete R216

1. DCON POWER -

Title: <Title>		
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