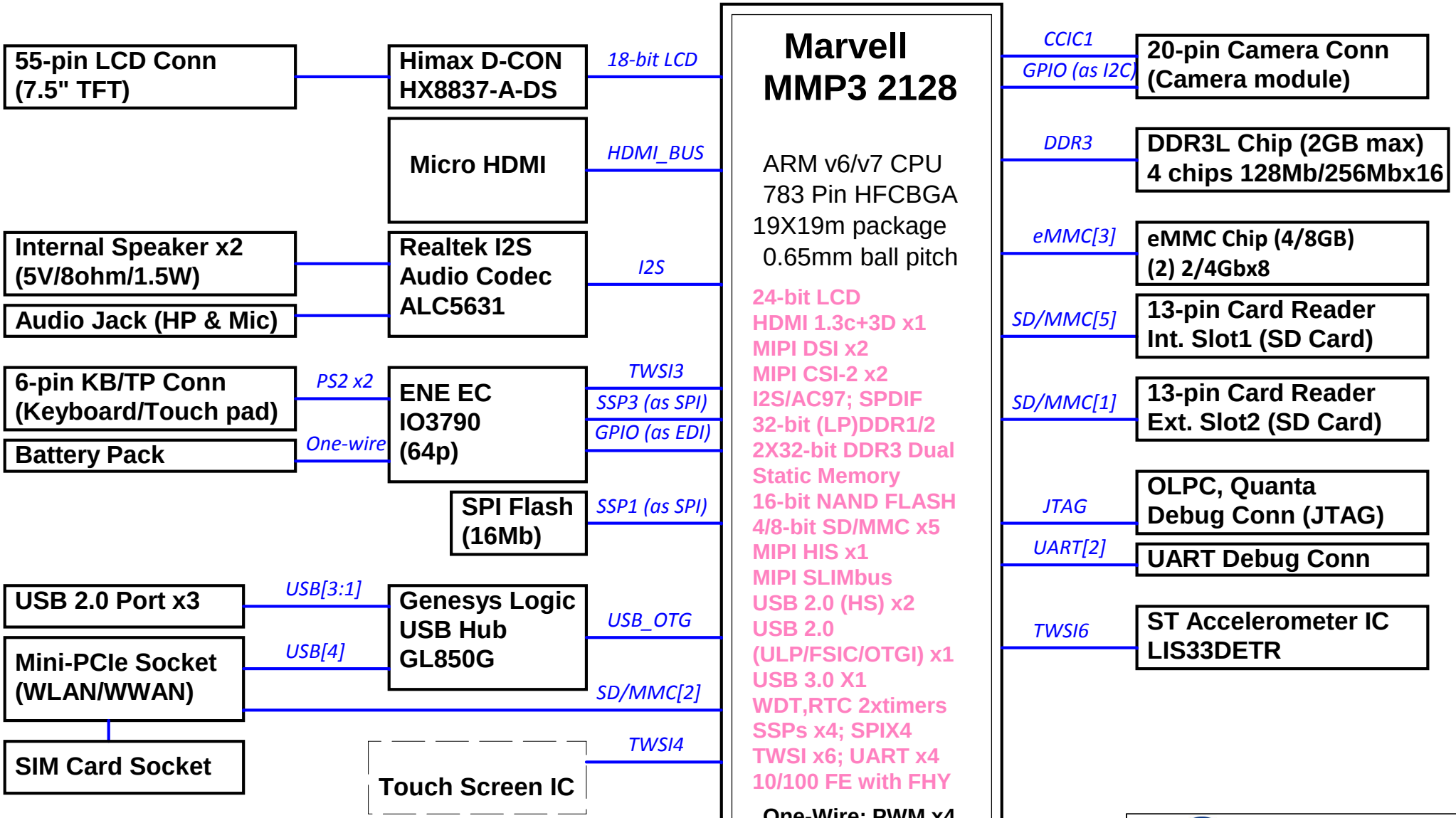
CL4 Preliminary Schematic (C2 Version, C phase)

Quanta Computer Inc.
PROJECT : CL4

Size	Document Number	Rev
	TITLE PAGE	1A

Date: Wednesday, January 30, 2013 Sheet 1 of 40

CL4 System Block Diagram (B Version, A2 stage)



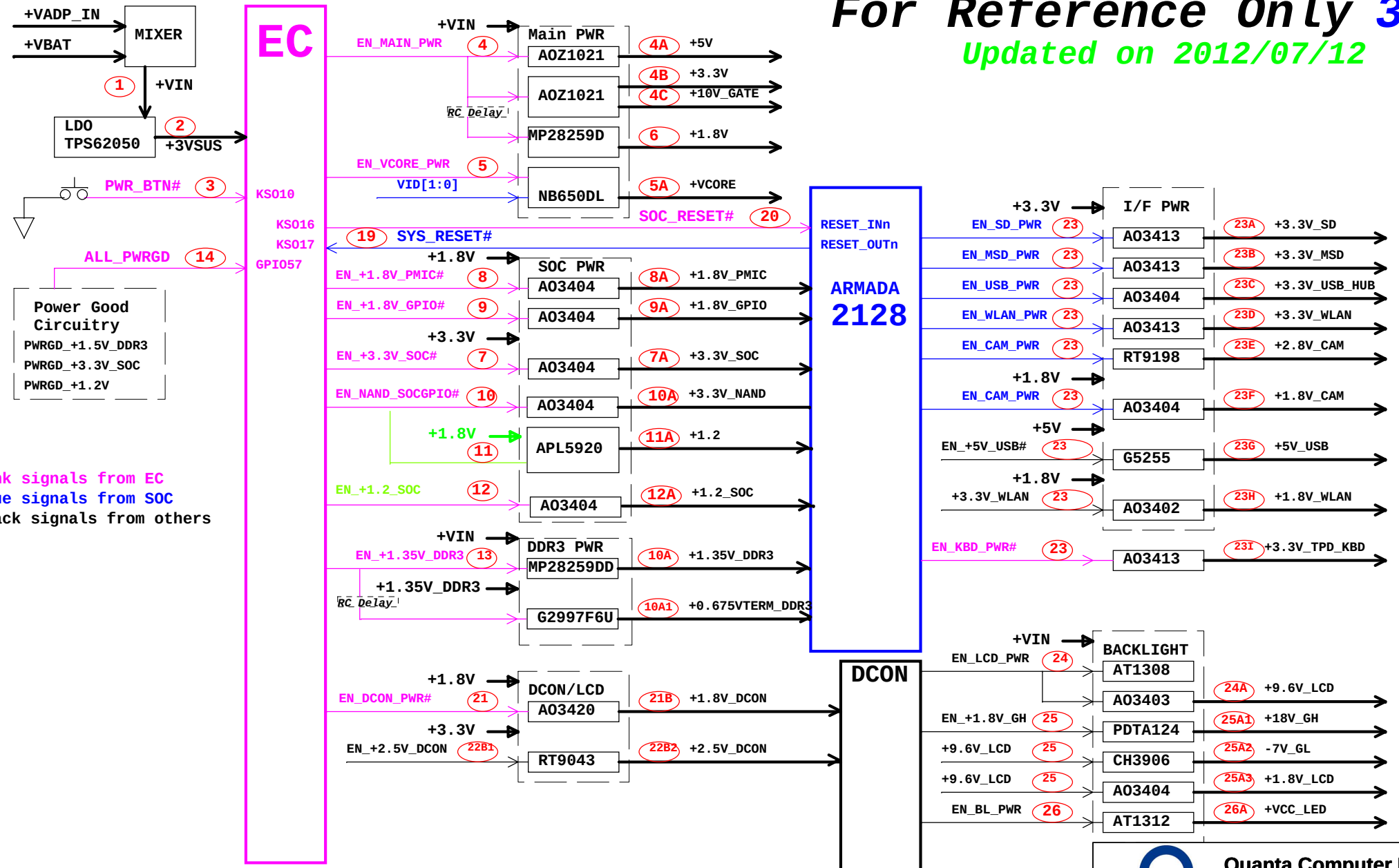
Quanta Computer Inc.
PROJECT : CL4

Size	Document Number	Rev
	SYSTEM BLOCK DIAGRAM	1A

Date: Wednesday, January 30, 2013 Sheet 2 of 40

For Reference Only 3

Updated on 2012/07/12



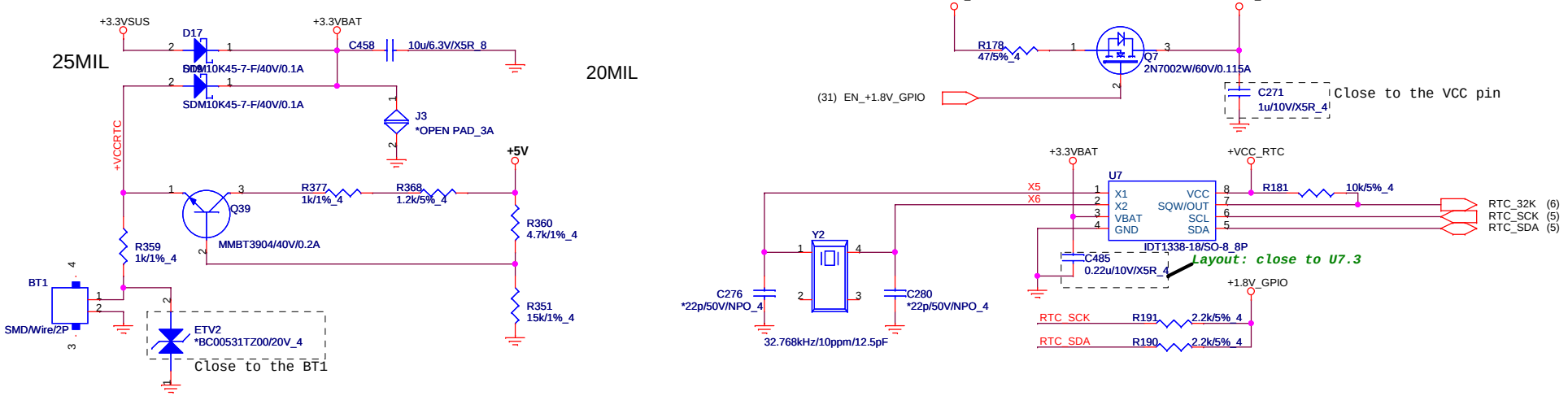
Quanta Computer Inc.

PROJECT : CL4

Size	Document Number	Rev
	POWER SEQUENCE	1A

Date: Wednesday, January 30, 2013 Sheet 3 of 40

RTC Battery Charger

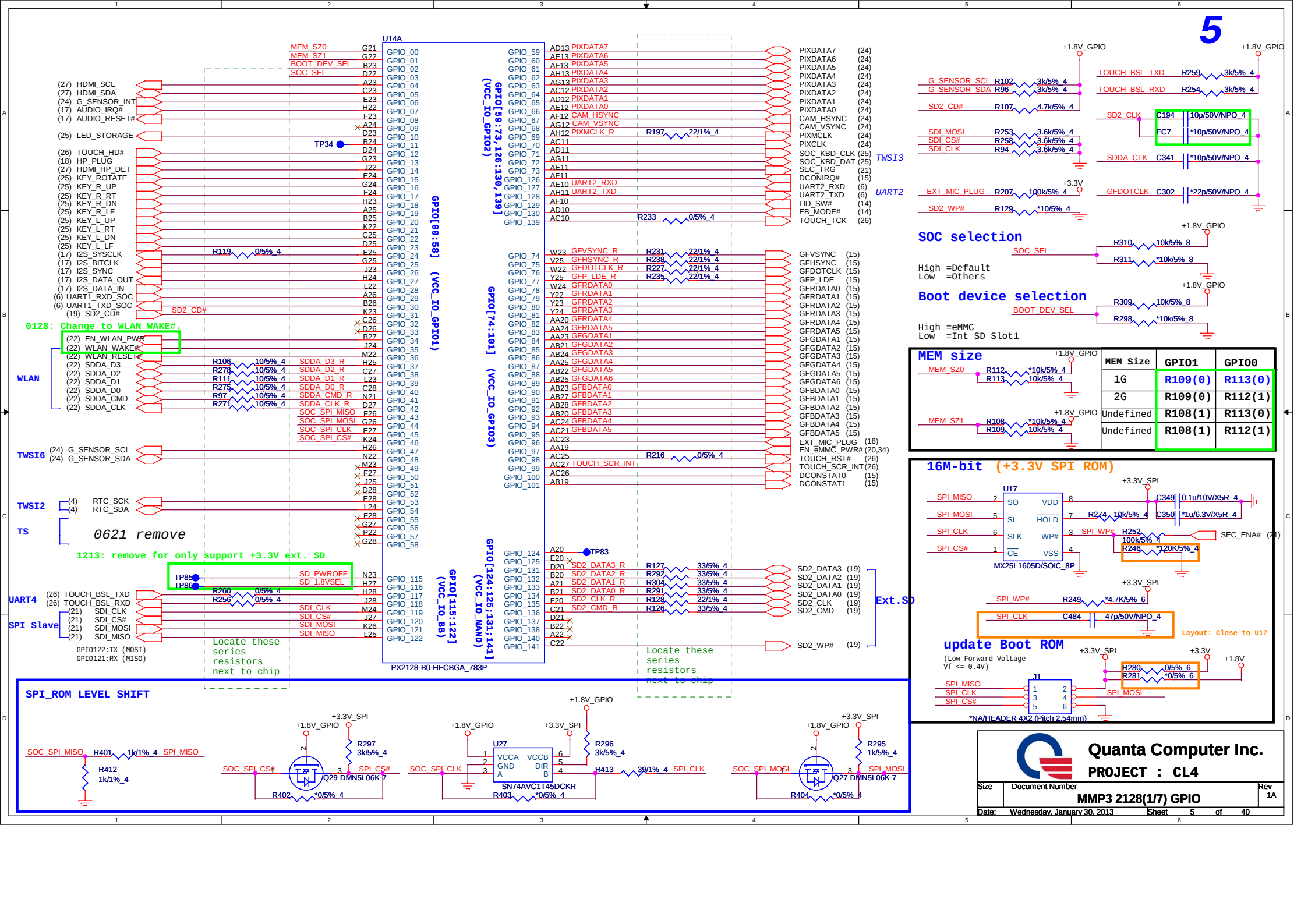


Quanta Computer Inc.

PROJECT : CL4

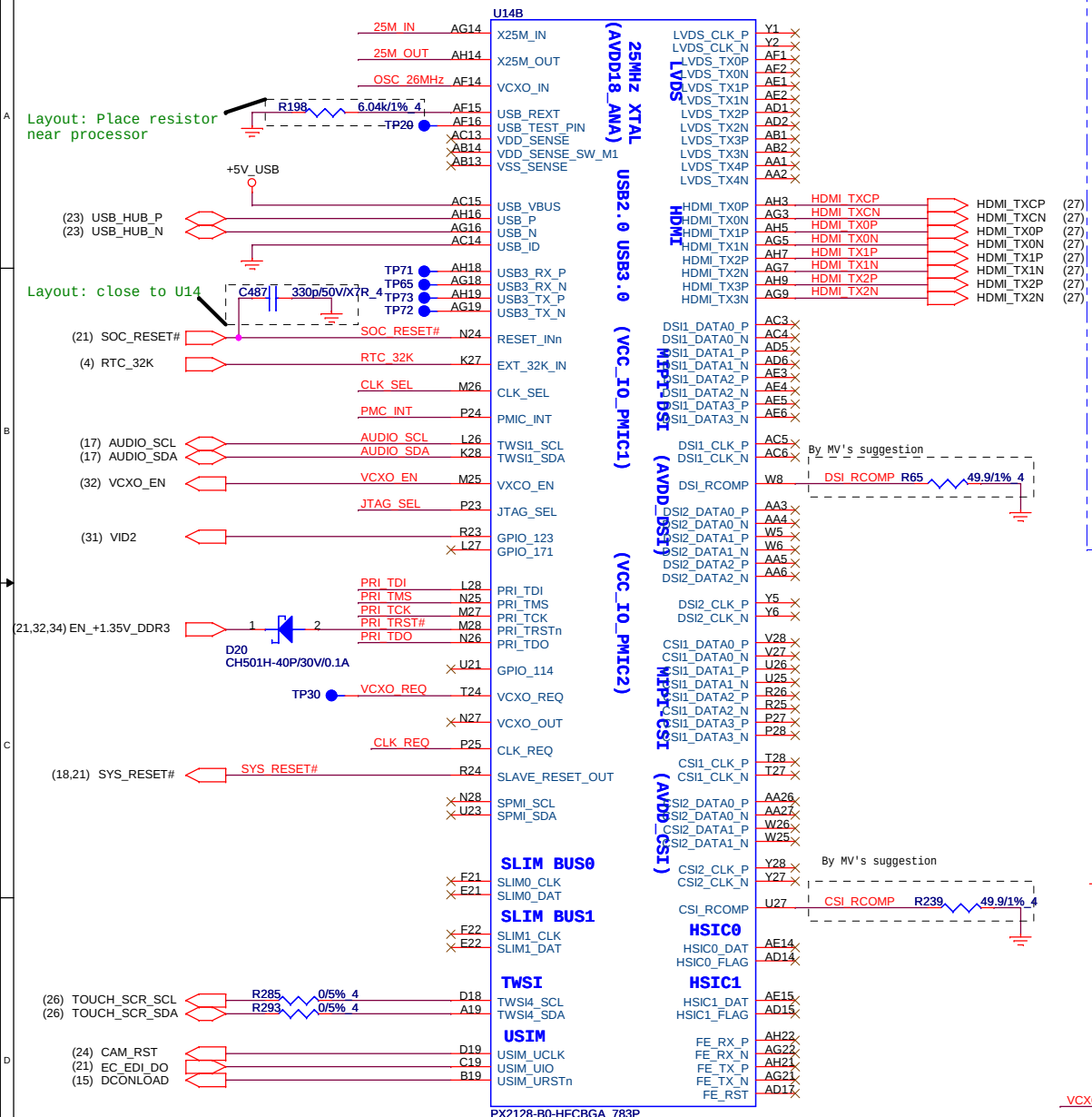
Size	Document Number	Rev
	RTC BATTERY & RTC CLOCK	1A

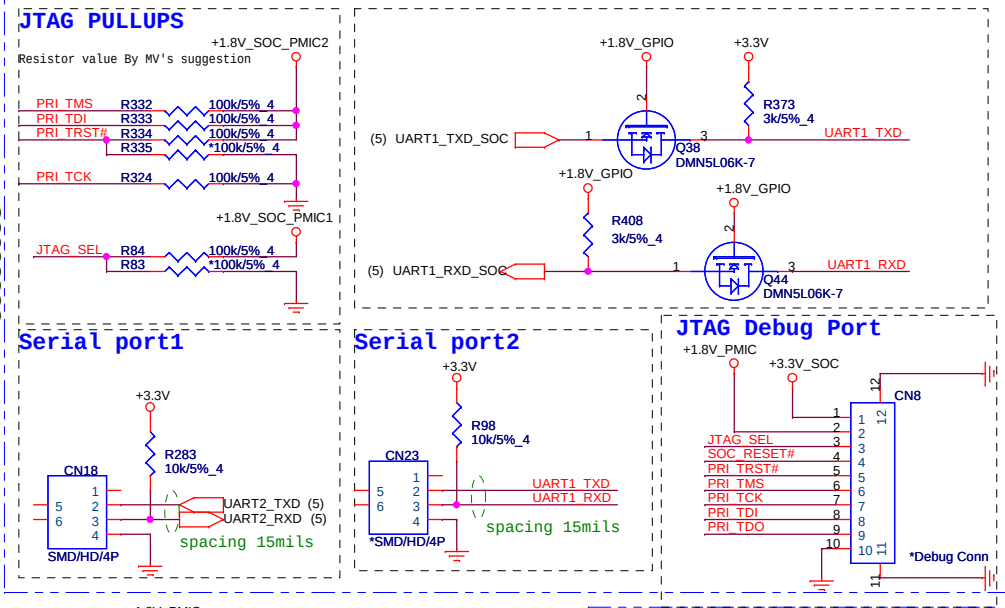
Date: Wednesday, January 30, 2013 Sheet 4 of 40

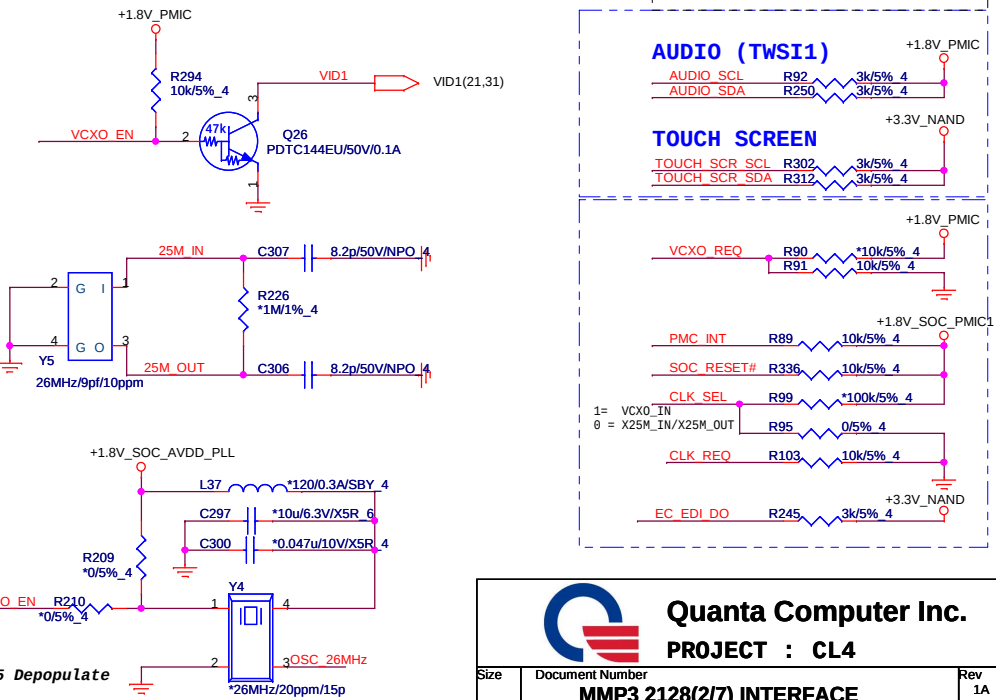

5
U14A
PX2128-B0-HFCBGA_783P
WLAN
TWSI6
TWSI2
TS
UART4
SPI Slave
0621 remove
1213: remove for only support +3.3V ext. SD
0128: Change to WLAN_WAKE#.
Locate these series resistors next to chip
SOC selection
High =Default
Low =Others
Boot device selection
High =eMMC
Low =Int SD Slot1
MEM size
MEM Size | GPIO1 | GPIO0
1G | R109(0) | R113(0)
2G | R109(0) | R112(1)
Undefined | R108(1) | R113(0)
Undefined | R108(1) | R112(1)
16M-bit (+3.3V SPI ROM)
MX25L1605D/SOIC_8P
update Boot ROM
(Low Forward Voltage Vf <= 0.4V)
*NA/HEADER 4X2 (Pitch 2.54mm)
Layout: Close to U17
SPI_ROM LEVEL SHIFT
SN74AVC1T45DCKR
Q29 DMN5L06K-7
Q27 DMN5L06K-7
Quanta Computer Inc.
PROJECT : CL4
MMP3 2128(1/7) GPIO
Size
Document Number
Rev 1A
Date: Wednesday, January 30, 2013
Sheet 5 of 40

JTAG & UART Debug Port

6





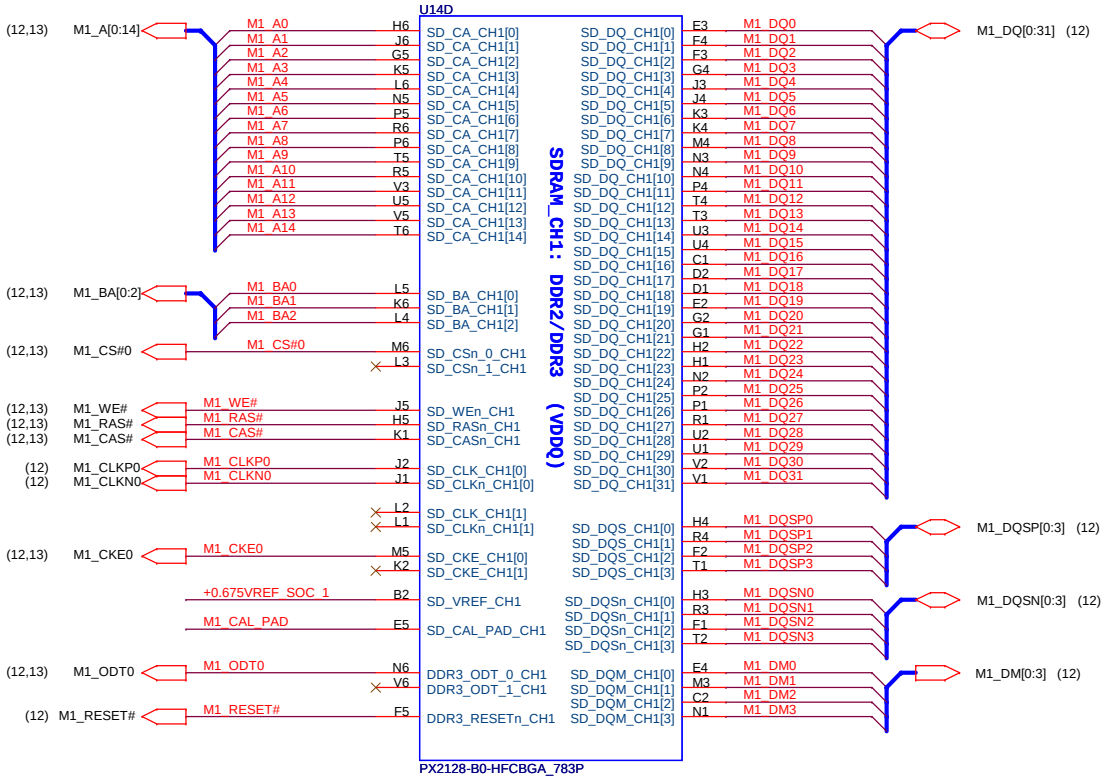


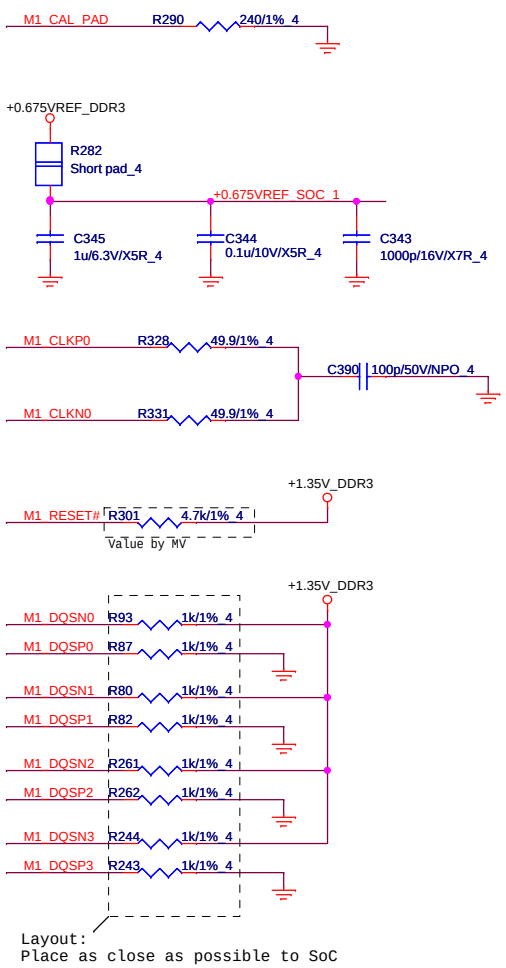
Quanta Computer Inc.

PROJECT : CL4

Size	Document Number	Rev
	MMP3 2128(2/7) INTERFACE	1A

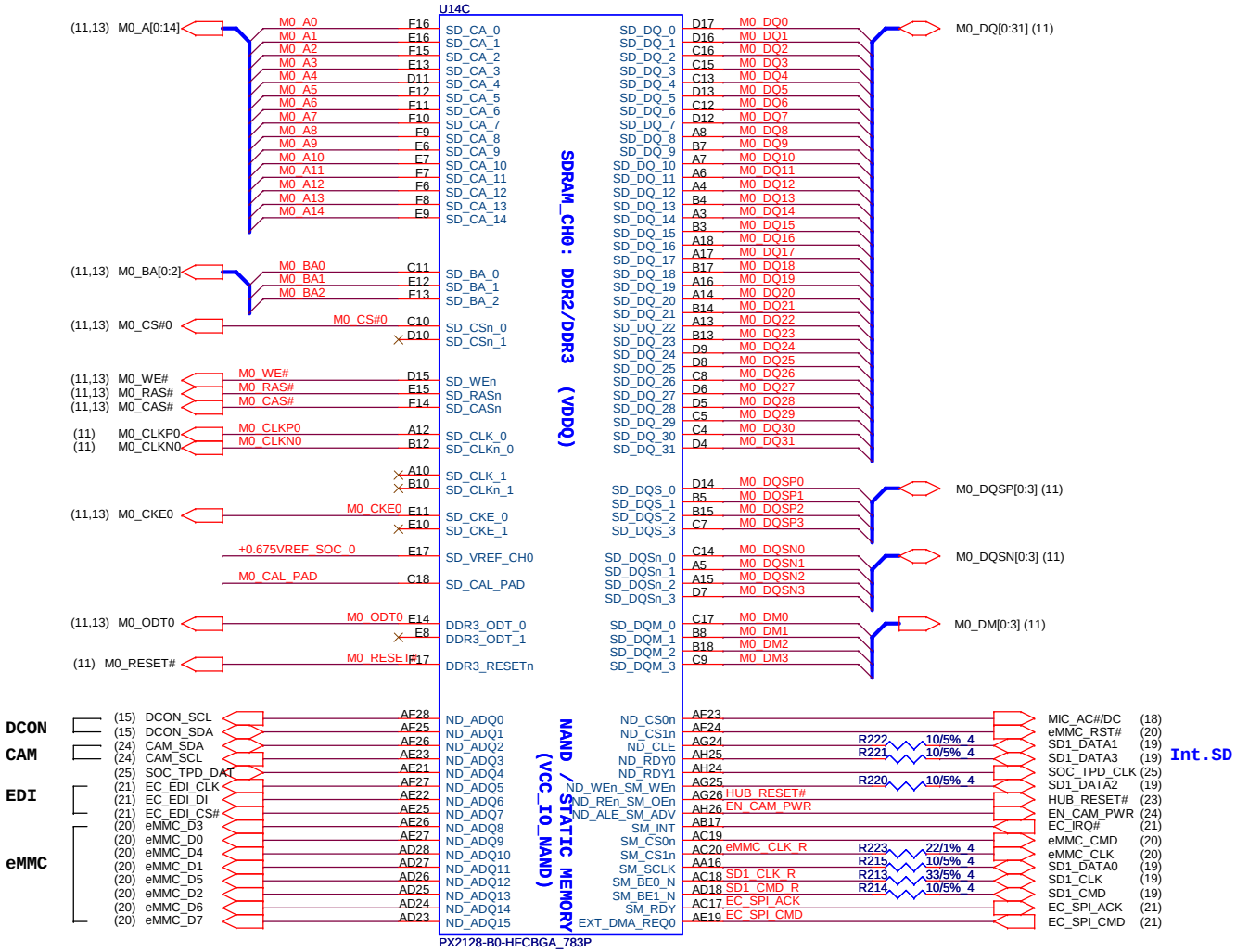
Date: Wednesday, January 30, 2013 Sheet 6 of 40

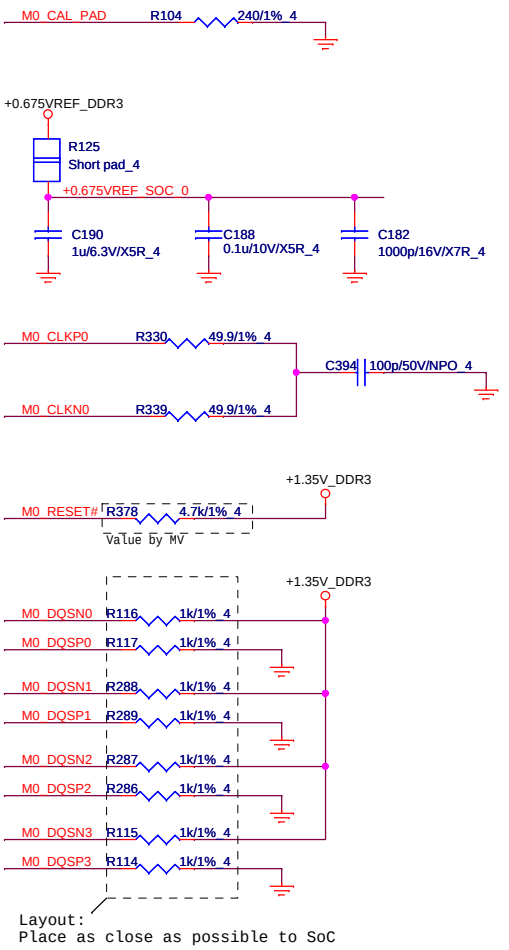


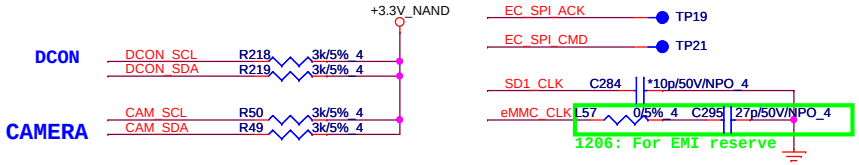


Quanta Computer Inc.
PROJECT : CL2

Size	Document Number	Rev
	ARMADA 610 (3/5) DDR3 & NAND	4A
Date: Wednesday, January 30, 2013	Sheet 7 of 40	



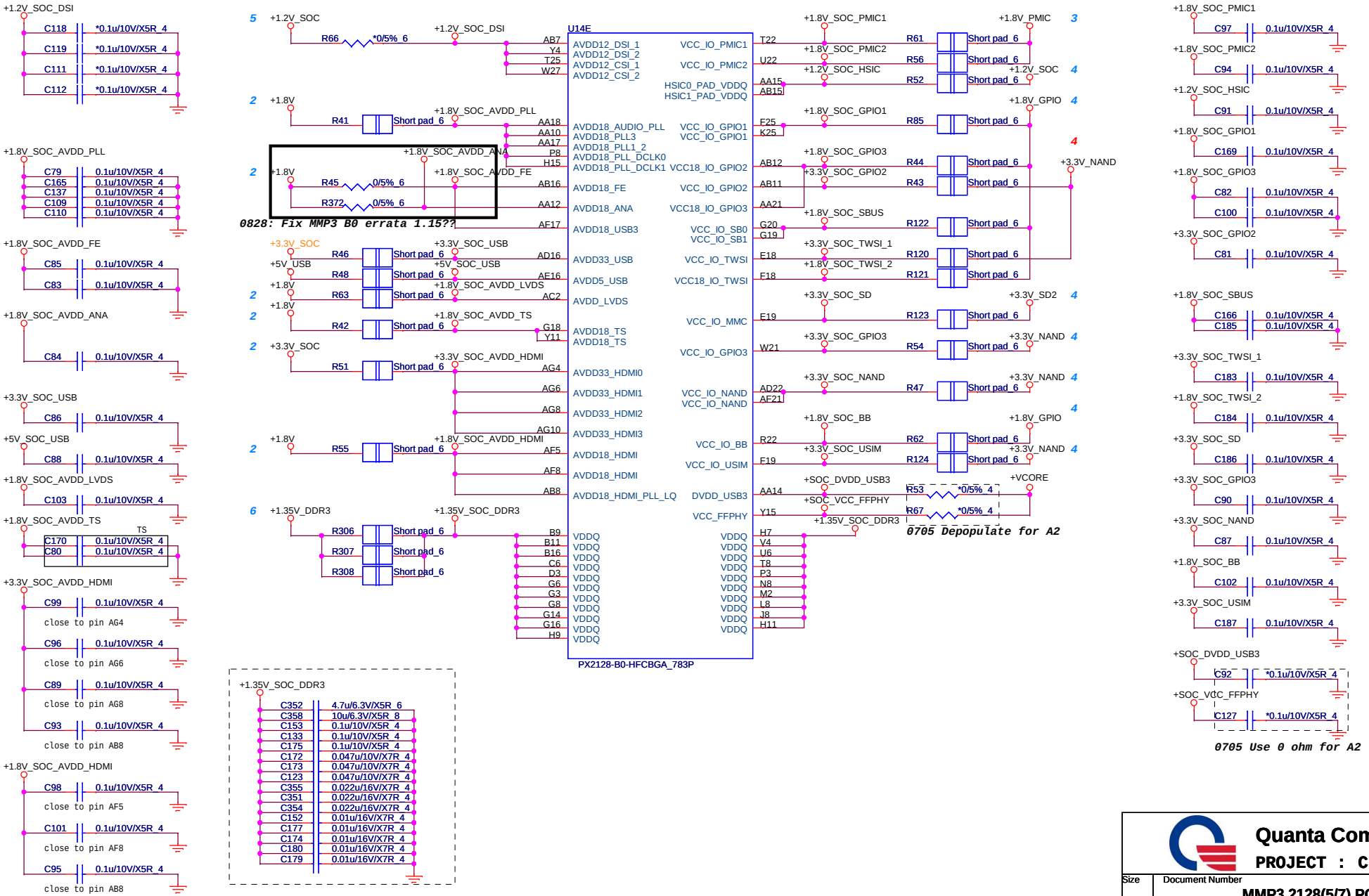




Quanta Computer Inc.
PROJECT : CL4

Size	Document Number	Rev
	MMP3 2128(3/7) DD3/NAND	1A

Date: Wednesday, January 30, 2013 Sheet 8 of 40

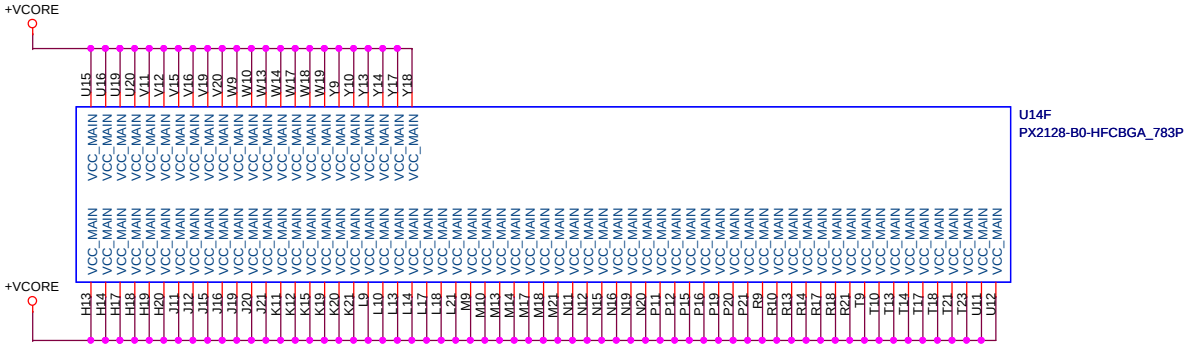


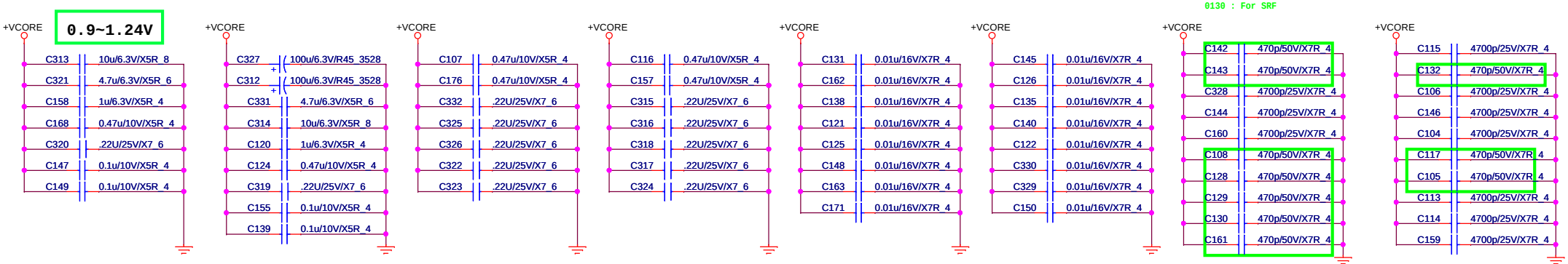
Quanta Computer Inc.

PROJECT : CL4

Size	Document Number	Rev
	MMP3 2128(5/7) POWER	1A

Date: Wednesday, January 30, 2013 Sheet 9 of 40



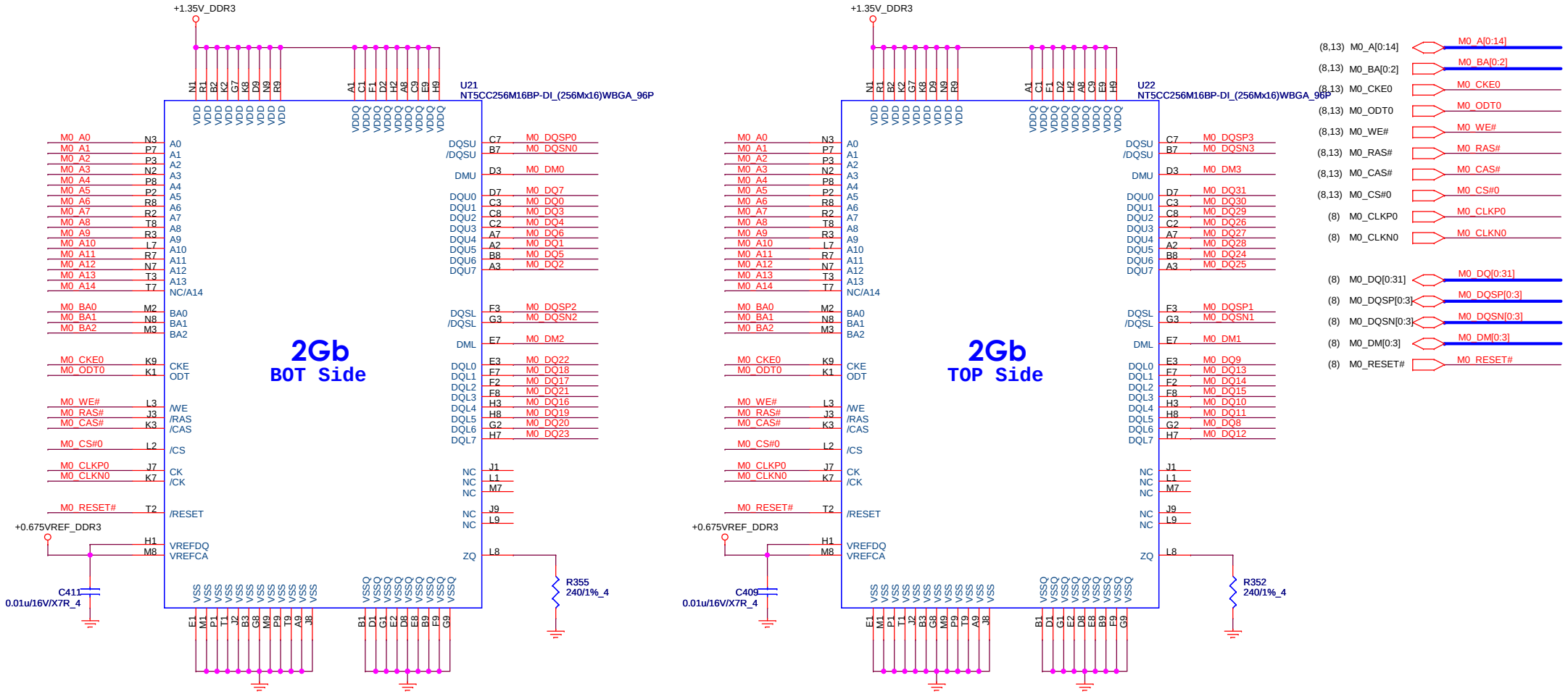


Quanta Computer Inc.

PROJECT : CL4

Size	Document Number	Rev
	MMP3 2128(6,7/7)VSS & +VCORE	1A

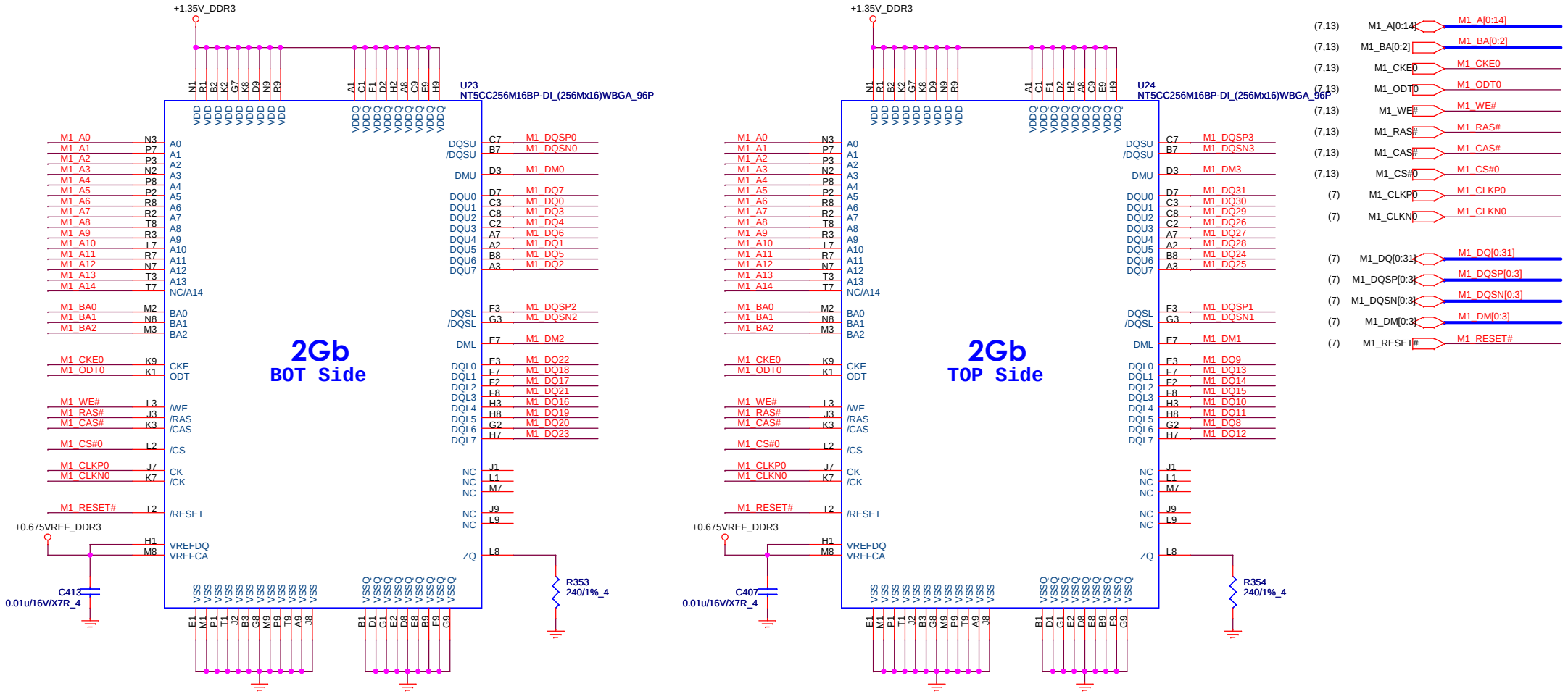
Date: Wednesday, January 30, 2013 Sheet 10 of 40



DDR3 SDRAM 96ball x16 list...

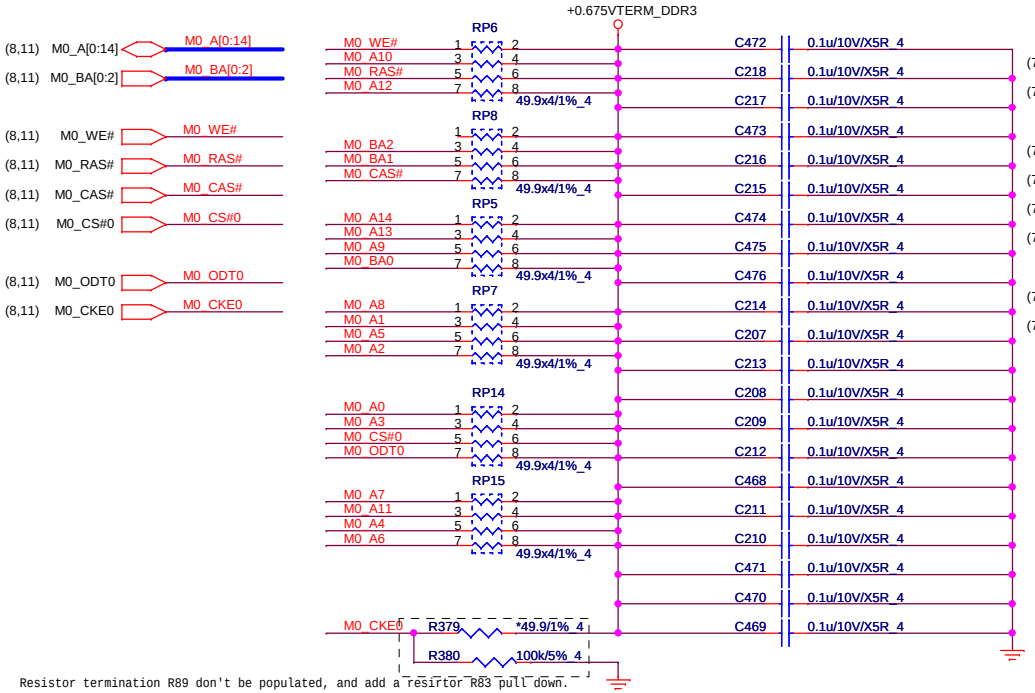
HYU -- 2Gb x16 -- AKD5MGGTW04 -- V

Quanta Computer Inc.		
PROJECT : CL3		
Size	Document Number: DDR3 SDRAM	Rev: 1A
Date: Wednesday, January 30, 2013	Sheet 11 of 40	



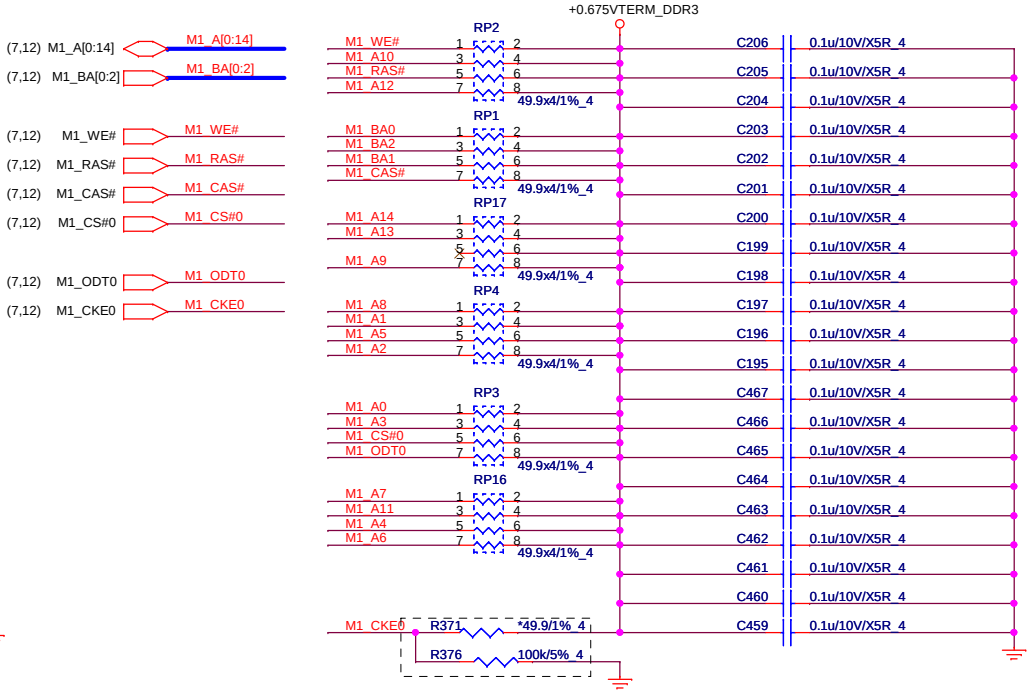
Quanta Computer Inc.		
PROJECT : CL3		
Size	Document Number: DDR3 SDRAM	Rev: 1A
Date: Wednesday, January 30, 2013	Sheet 12 of 40	

CH0 Address/Control/Clock Terminations



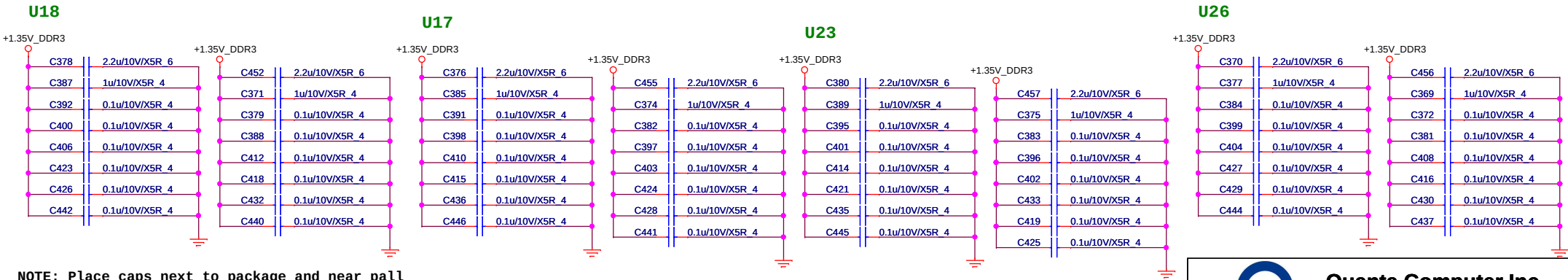
Resistor termination R89 don't be populated, and add a resirtor R83 pull down.

CH1 Address/Control/Clock Terminations



DDR3 Power Decoupling

Follow Marvell's schematic



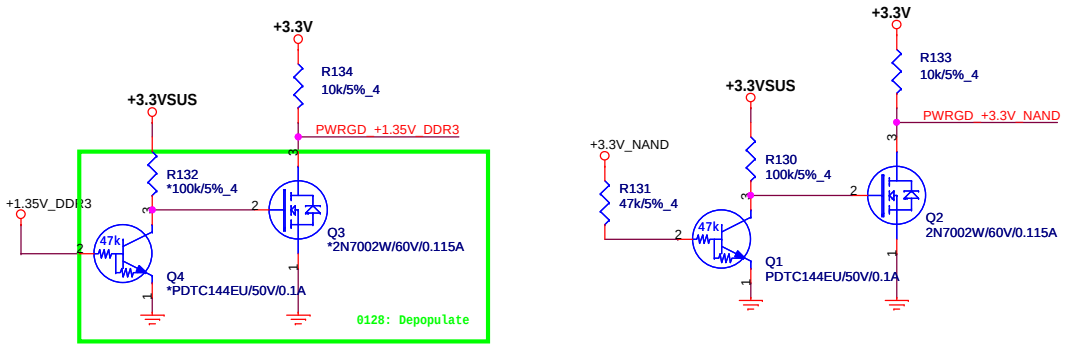
NOTE: Place caps next to package and near pall

Quanta Computer Inc.

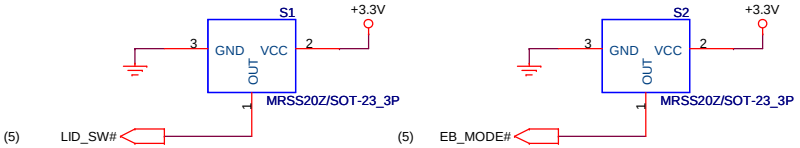
PROJECT : CL4

Size	Document Number	Rev
	DDR3 TERMINATION	1A
Date: Wednesday, January 30, 2013	Sheet 13 of 40	

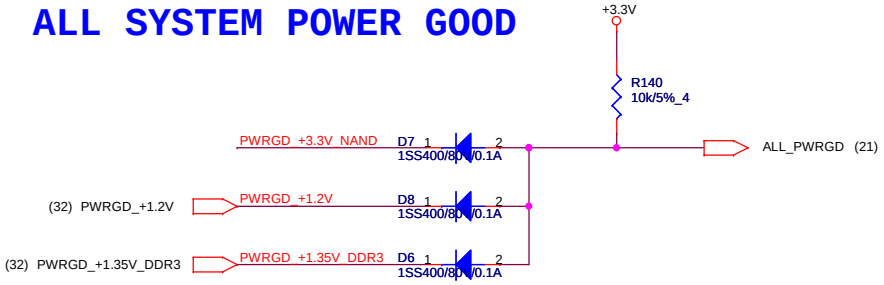
POWER GOOD



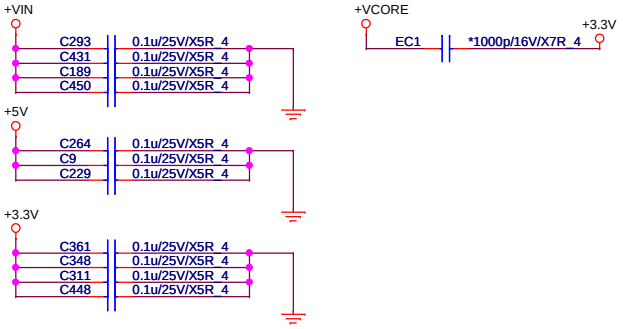
MR Sensor



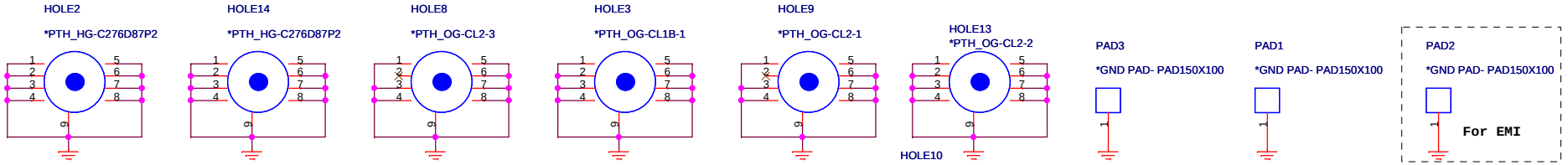
ALL SYSTEM POWER GOOD



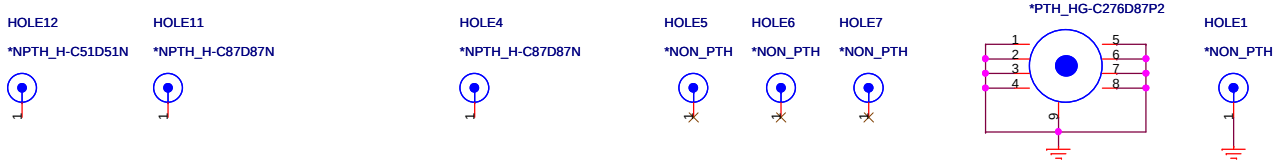
EMI request



Screw Hole



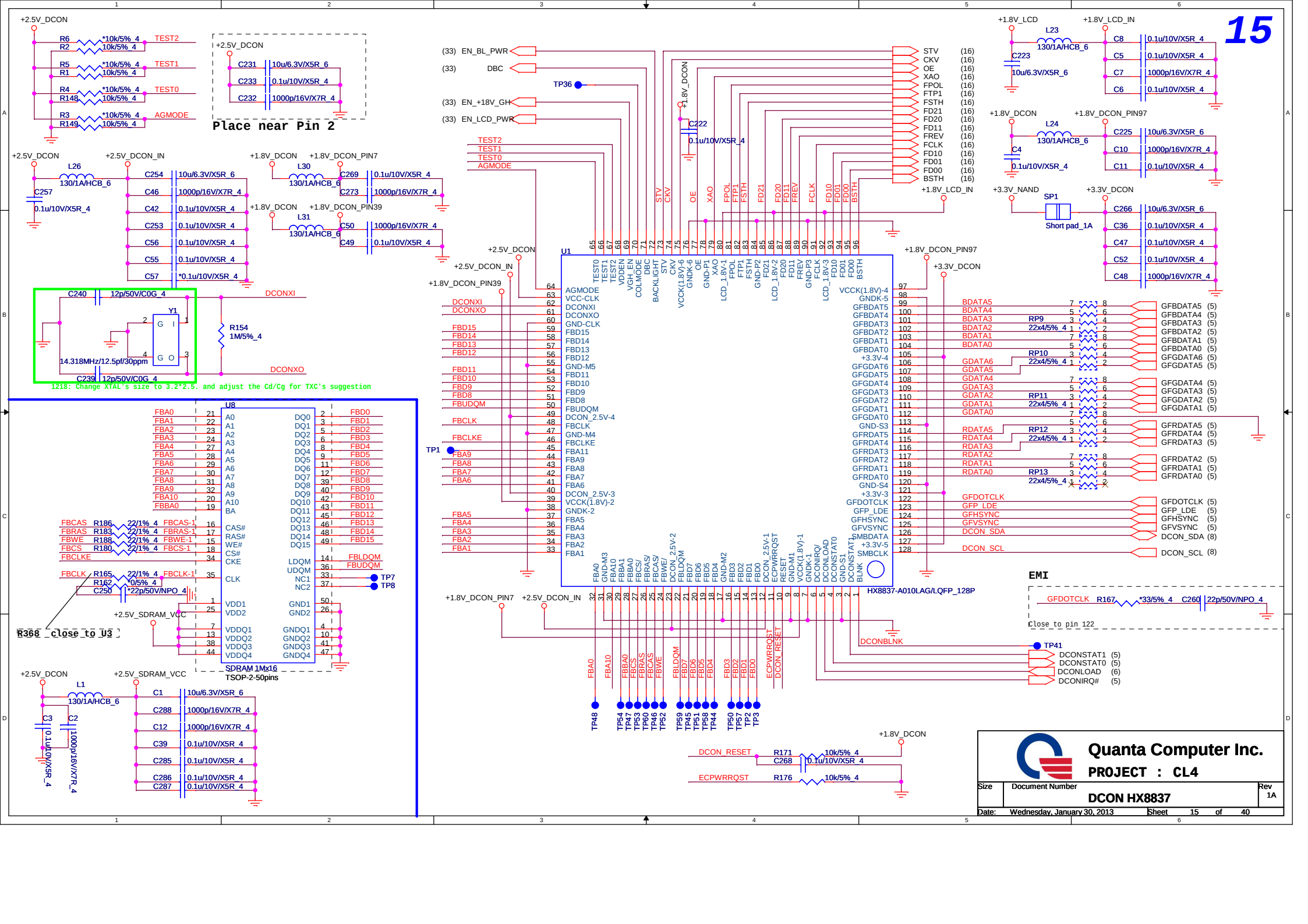
NPTH

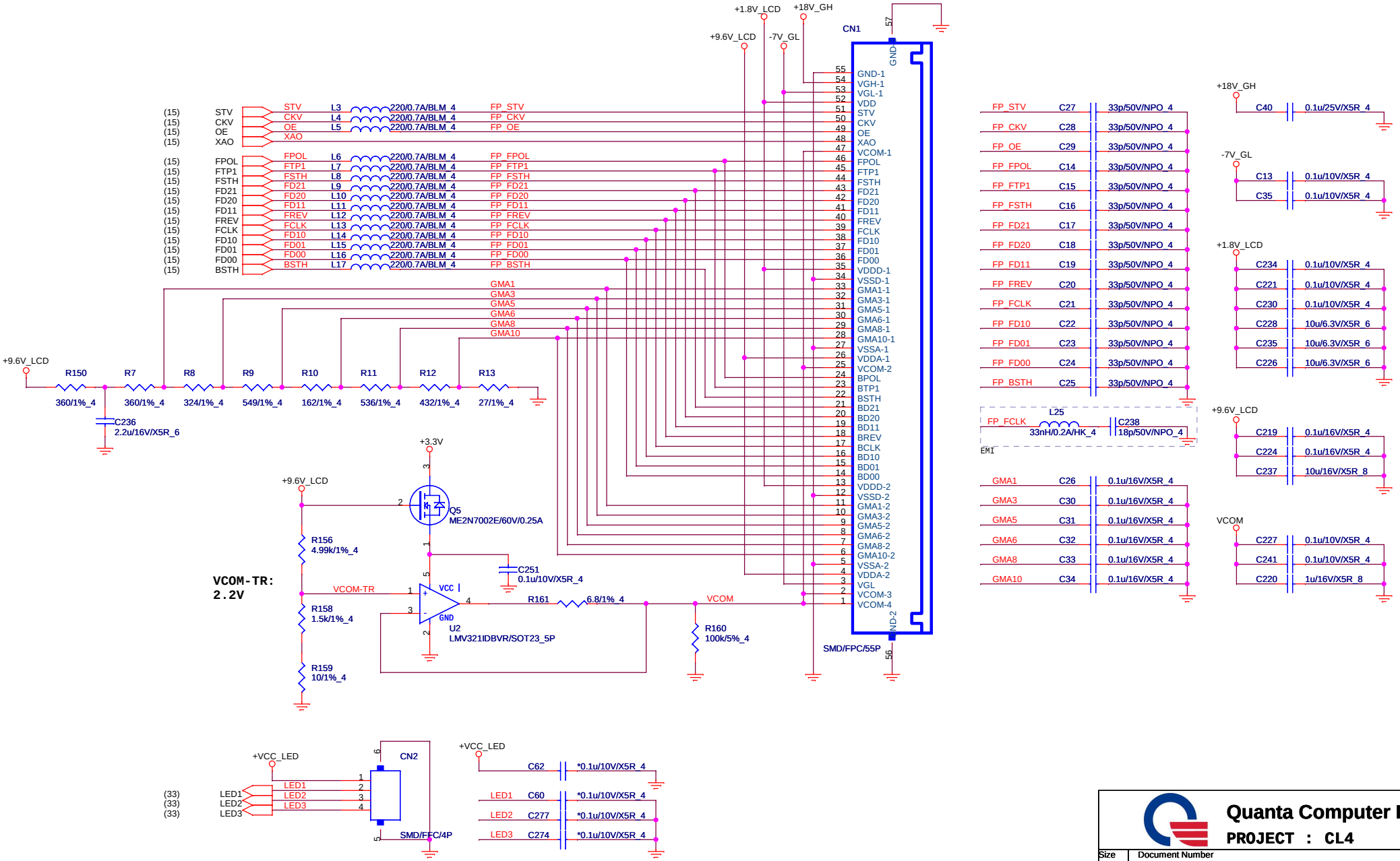


Quanta Computer Inc.
PROJECT : CL4

Size	Document Number	Rev
	RESET CIRCUIT/HOLES	1A

Date: Wednesday, January 30, 2013 Sheet 14 of 40


15
+2.5V_DCON
R6 *10k/5%_4
R2 10k/5%_4
TEST2
R5 *10k/5%_4
R1 10k/5%_4
TEST1
R4 *10k/5%_4
R148 10k/5%_4
TEST0
R3 *10k/5%_4
R149 10k/5%_4
AGMODE
C231 10u/6.3V/X5R_6
C233 0.1u/10V/X5R_4
C232 1000p/16V/X7R_4
Place near Pin 2
+2.5V_DCON
+2.5V_DCON_IN
L26 130/1A/HCB_6
C257 0.1u/10V/X5R_4
C254 10u/6.3V/X5R_6
C46 1000p/16V/X7R_4
C42 0.1u/10V/X5R_4
C253 0.1u/10V/X5R_4
C56 0.1u/10V/X5R_4
C55 0.1u/10V/X5R_4
C57 *0.1u/10V/X5R_4
+1.8V_DCON
+1.8V_DCON_PIN7
L30 130/1A/HCB_6
C269 0.1u/10V/X5R_4
C273 1000p/16V/X7R_4
+1.8V_DCON
+1.8V_DCON_PIN39
L31 130/1A/HCB_6
C50 1000p/16V/X7R_4
C49 0.1u/10V/X5R_4
C240 12p/50V/C0G_4
Y1
14.318MHz/12.5pf/30ppm
C239 12p/50V/C0G_4
DCONXI
DCONXO
R154 1M/5%_4
1218: Change XTAL's size to 3.2*2.5. and adjust the Cd/Cg for TXC's suggestion
U8
FBA0 FBA1 FBA2 FBA3 FBA4 FBA5 FBA6 FBA7 FBA8 FBA9 FBA10 FBBA0
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 BA
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
FBD0 FBD1 FBD2 FBD3 FBD4 FBD5 FBD6 FBD7 FBD8 FBD9 FBD10 FBD11 FBD12 FBD13 FBD14 FBD15
FBCAS R186 22/1%_4 FBCAS-1
FBRAS R183 22/1%_4 FBRAS-1
FBWE R188 22/1%_4 FBWE-1
FBCS R180 22/1%_4 FBCS-1
FBCLKE
FBCLK R165 22/1%_4 FBCLK-1
R162 *0/5%_4
C250 *22p/50V/NPO_4
CS# CKE CLK
LDQM UDQM NC1 NC2
FBLDQM FBUDQM
TP7 TP8
VDD1 VDD2 VDDQ1 VDDQ2 VDDQ3 VDDQ4
GND1 GND2 GNDQ1 GNDQ2 GNDQ3 GNDQ4
+2.5V_SDRAM_VCC
R368 close to U3
SDRAM 1Mx16
TSOP-2-50pins
+2.5V_DCON
L1 130/1A/HCB_6
C3 0.1u/10V/X5R_4
C2 1000p/16V/X7R_4
+2.5V_SDRAM_VCC
C1 10u/6.3V/X5R_6
C288 1000p/16V/X7R_4
C12 1000p/16V/X7R_4
C39 0.1u/10V/X5R_4
C285 0.1u/10V/X5R_4
C286 0.1u/10V/X5R_4
C287 0.1u/10V/X5R_4
(33) EN_BL_PWR
(33) DBC
TP36
(33) EN_+18V_GH
(33) EN_LCD_PWR
TEST2 TEST1 TEST0 AGMODE
+1.8V_DCON
C222 0.1u/10V/X5R_4
U1
AGMODE VCC-CLK DCONXI DCONXO GND-CLK FBD15 FBD14 FBD13 FBD12 FBD11 FBD10 FBD9 FBD8 FBUDQM DCON_2.5V-4 FBCLK GND-M4 FBCLKE FBA11 FBA9 FBA8 FBA7 FBA6 DCON_2.5V-3 VCCK(1.8V)-2 GNDK-2 FBA5 FBA4 FBA3 FBA2 FBA1
TEST0 TEST1 TEST2 VDDEN VGH_EN COLMODE DBC BACKLIGHT STV CKV VCCK(1.8V)-6 GNDK-6 OE GND-P1 XAO LCD_1.8V-1 FPOL FTP1 FSTH GND-P2 FD21 LCD_1.8V-2 FD20 FD11 FREV GND-P3 FCLK LCD_1.8V-3 FD10 FD01 FD00 BSTH
VCCK(1.8V)-4 GNDK-5 GFBDAT5 GFBDAT4 GFBDAT3 GFBDAT2 GFBDAT1 GFBDAT0 +3.3V-4 GFGDAT6 GFGDAT5 GFGDAT4 GFGDAT3 GFGDAT2 GFGDAT1 GFGDAT0 GND-S3 GFRDAT5 GFRDAT4 GFRDAT3 GFRDAT2 GFRDAT1 GFRDAT0 GND-S4 +3.3V-3 GFDOTCLK GFP_LDE GFHSYNC GFVSYNC SMBDATA +3.3V-5 SMBCLK
GFDOTCLK GFP_LDE GFHSYNC GFVSYNC DCON_SDA DCON_SCL
GND-M3 FBA10 FBBA0 FBA1 FBCS/ FBRAS/ FBCAS/ FBWE/ DCON_2.5V-2 FBLDQM FBD7 FBD6 FBD5 FBD4 GND-M2 FBD3 FBD2 FBD1 FBD0 DCON_2.5V-1 ECPWRRQST RESET GND-M1 VCCK(1.8V)-1 GNDK-1 DCONIRQ/ DCONLOAD DCONSTAT0 GND-S1 DCONSTAT1 BLNK
HX8837-A010LAG/LQFP_128P
STV CKV OE XAO FPOL FTP1 FSTH FD21 FD20 FD11 FREV FCLK FD10 FD01 FD00 BSTH
+1.8V_LCD_IN
+1.8V_LCD
L23 130/1A/HCB_6
C223 10u/6.3V/X5R_6
C8 0.1u/10V/X5R_4
C5 0.1u/10V/X5R_4
C7 1000p/16V/X7R_4
C6 0.1u/10V/X5R_4
+1.8V_DCON
+1.8V_DCON_PIN97
L24 130/1A/HCB_6
C4 0.1u/10V/X5R_4
C225 10u/6.3V/X5R_6
C10 1000p/16V/X7R_4
C11 0.1u/10V/X5R_4
+3.3V_NAND
SP1 Short pad_1A
+3.3V_DCON
C266 10u/6.3V/X5R_6
C36 0.1u/10V/X5R_4
C47 0.1u/10V/X5R_4
C52 0.1u/10V/X5R_4
C48 1000p/16V/X7R_4
+1.8V_DCON_PIN97
+3.3V_DCON
BDATA5 BDATA4 BDATA3 BDATA2 BDATA1 BDATA0
RP9 22x4/5%_4
RP10 22x4/5%_4
GDATA6 GDATA5 GDATA4 GDATA3 GDATA2 GDATA1 GDATA0
RP11 22x4/5%_4
RP12 22x4/5%_4
RDATA5 RDATA4 RDATA3 RDATA2 RDATA1 RDATA0
RP13 22x4/5%_4
GFBDATA5 (5) GFBDATA4 (5) GFBDATA3 (5) GFBDATA2 (5) GFBDATA1 (5) GFBDATA0 (5) GFGDATA6 (5) GFGDATA5 (5)
GFGDATA4 (5) GFGDATA3 (5) GFGDATA2 (5) GFGDATA1 (5)
GFRDATA5 (5) GFRDATA4 (5) GFRDATA3 (5)
GFRDATA2 (5) GFRDATA1 (5) GFRDATA0 (5)
GFDOTCLK (5) GFP_LDE (5) GFHSYNC (5) GFVSYNC (5) DCON_SDA (8) DCON_SCL (8)
EMI
GFDOTCLK R167 *33/5%_4 C260 22p/50V/NPO_4
Close to pin 122
TP1
TP41
DCONSTAT1 (5) DCONSTAT0 (5) DCONLOAD (6) DCONIRQ# (5)
DCONBLNK
TP48 TP54 TP47 TP53 TP60 TP46 TP52 TP59 TP45 TP51 TP58 TP44 TP50 TP57 TP2 TP3
DCON_RESET R171 10k/5%_4 C268 0.1u/10V/X5R_4
ECPWRRQST R176 10k/5%_4
+1.8V_DCON
Quanta Computer Inc.
PROJECT : CL4
Size
Document Number
DCON HX8837
Rev 1A
Date: Wednesday, January 30, 2013
Sheet 15 of 40



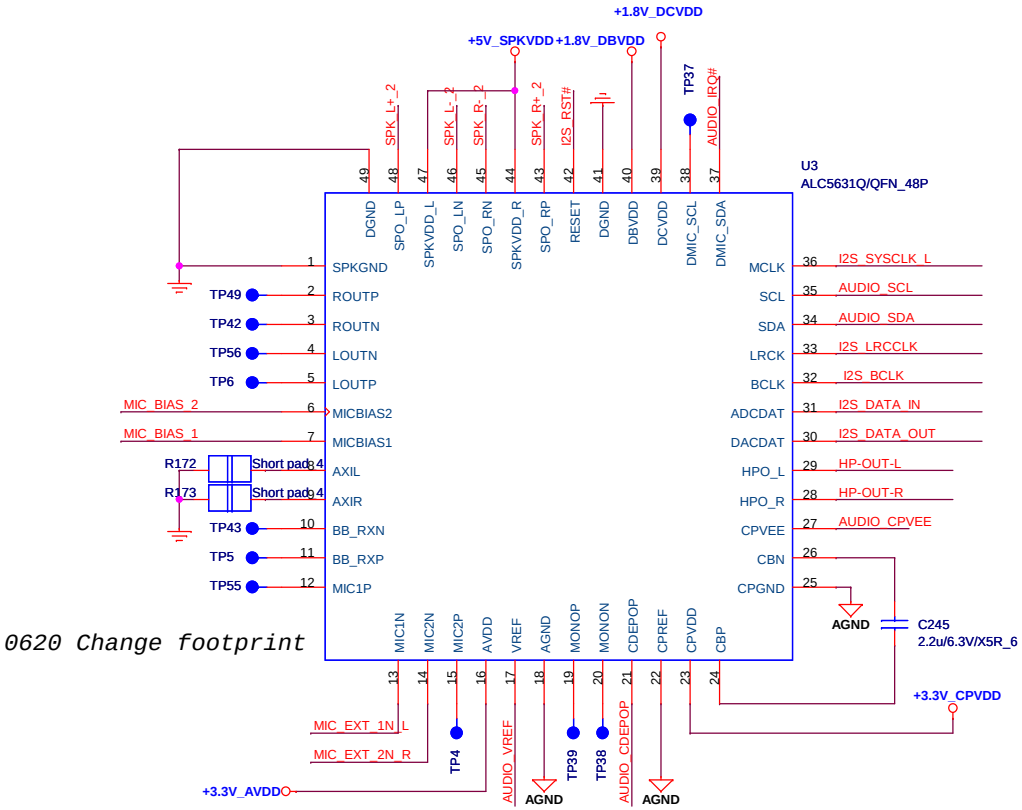
Quanta Computer Inc.

PROJECT : CL4

Size	Document Number	Rev
	LCD CONNECTOR	1A

Date: Wednesday, January 30, 2013 Sheet 16 of 40

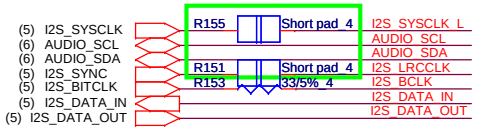
AUDIO CODEC



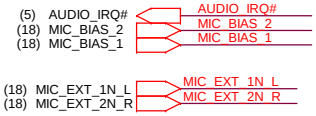
0620 Change footprint

I2S:

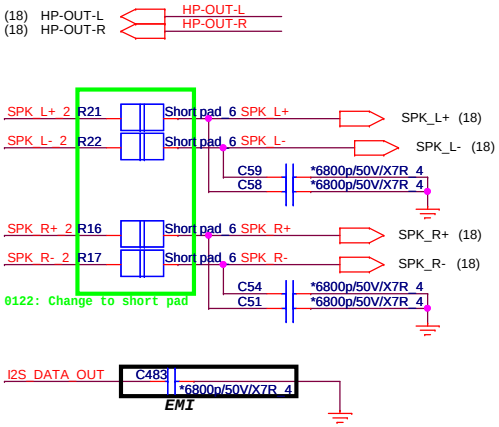
0122: Change to short pad



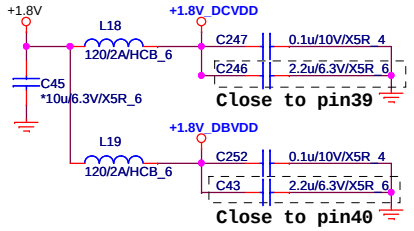
INT/EXT MIC:

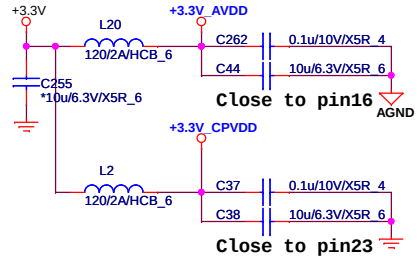


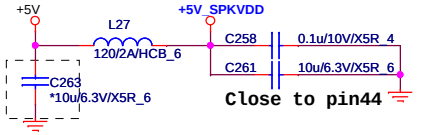
H/P OUT & SPK OUT:



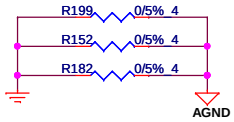
Audio Power



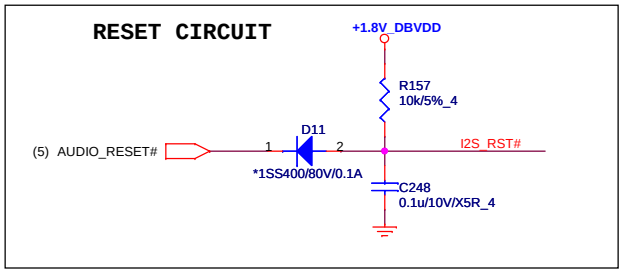


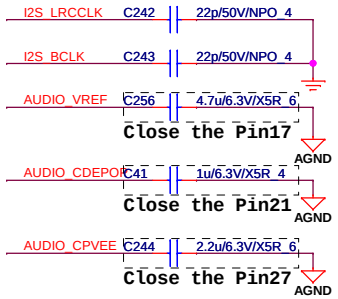


Analog Ground of Audio



RESET CIRCUIT





Quanta Computer Inc.

PROJECT : CL4

Size	Document Number	Rev
	I2S AUDIO CODEC ALC5631Q	1A

Date: Wednesday, January 30, 2013 Sheet 17 of 40

Head Phone Jack

ESD

D2
AZ5125-02/5V_SOT23-3L

C65 0.1u/10V/X5R_4 R193 22/1%_4
C72 0.1u/10V/X5R_4 R20 22/1%_4

Realtek suggest!!

(17) HP-OUT-L
(17) HP-OUT-R
HP-OUT-L
HP-OUT-R
R409 22/5%_8
R410 22/5%_8
L22 600/0.2A/BK_6
L21 600/0.2A/BK_6
HP-OUT-L_2
HP-OUT-R_2

1017: to fix headphone overvoltage test

+1.8V_GPIO
R26 100k/5%_4
(5) HP_PLUG
HP_PLUG_1

CN4
DIP/6P_Audio Jack

Normal close type
Jack insert open

Internal Speaker Connectors

CN16
SMD/Wire/2P

(17) SPK_R+
(17) SPK_R-
R251 1/1%_6
R247 1/1%_6
SPK_R+_1
SPK_R-_1
C333 6800p/50V/X7R_4
C334 6800p/50V/X7R_4

CN17
SMD/Wire/2P

(17) SPK_L+
(17) SPK_L-
R78 1/1%_6
R81 1/1%_6
SPK_L+_1
SPK_L-_1
C151 6800p/50V/X7R_4
C134 6800p/50V/X7R_4

Microphone Jack

ESD

D13
BAT54S-7-F/30V/0.2A
D12
BAT54S-7-F/30V/0.2A

(17) MIC_BIAS_2
(17) MIC_BIAS_1
R23 2k/1%_4
R20 2k/1%_4
R177 680/1%_4
R179 680/1%_4
C61 4.7u/6.3V/X5R_6
C63 4.7u/6.3V/X5R_6

MIC_EXT_L
MIC_EXT_R
R184 470/5%_8
R170 470/5%_8
EXT_MIC_L_1
EXT_MIC_R_1
L32 600/0.2A/BK_6
L28 600/0.2A/BK_6
C270 100p/50V/NPO_4
C275 100p/50V/NPO_4
EXT_MIC_L_2
EXT_MIC_R_2

CN3
DIP/6P_Audio Jack

Normal close type
Jack insert open

+3.3V_NAND
R14 68/5%_4
LED2 GREEN
MIC Indicator
Q6
AO3416/20V/6.5A
EXT_MIC_PLUG

(6,21) SYS_RESET#
D10
*1SS400/80V/0.1A

MIC_BIAS_1
R164 10k/5%_4
R163 100k/5%_4
C249 470p/50V/X7R_4
R166 220k/5%_4
(5) EXT_MIC_PLUG

Internal Microphone

C64 100p/50V/NPO_4
CN6
CONN_MIC
ETV1
*BC00531TZ00/20V_4

MIC_EXT_L
C267 1u/10V/X5R_4
MIC_EXT_1N_L (17)
+3.3V_AVDD
U6
A Vcc
B
GND C
C272 1u/10V/X5R_4
MIC_AC#/DC (8)
SN74LVC1G66-Q1

MIC_EXT_R
C265 1u/10V/X5R_4
MIC_EXT_2N_R (17)
+3.3V_AVDD
U4
A Vcc
B
GND C
C259 1u/10V/X5R_4
MIC_AC#/DC
SN74LVC1G66-Q1

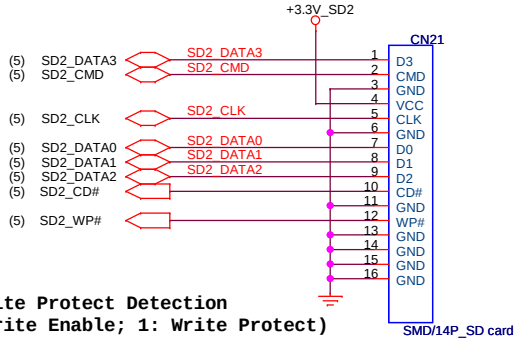
MIC_AC#/DC EC3 330p/50V/X7R_4
1227:EMI request

HIGH: DC Coupling
LOW: AC Coupling

Quanta Computer Inc.
PROJECT : CL4

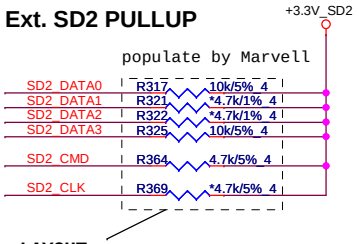
Size	Document Number	Rev
	AUDIO JACKS	1A
Date: Wednesday, January 30, 2013	Sheet 18 of 40	

Ext. SD2 Card Reader

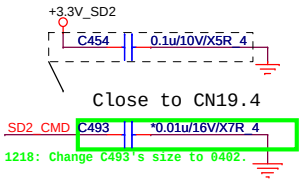


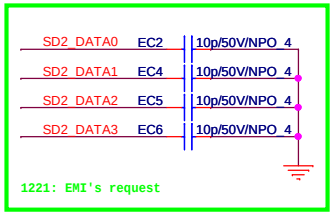
SD Write Protect Detection
(0: Write Enable; 1: Write Protect)

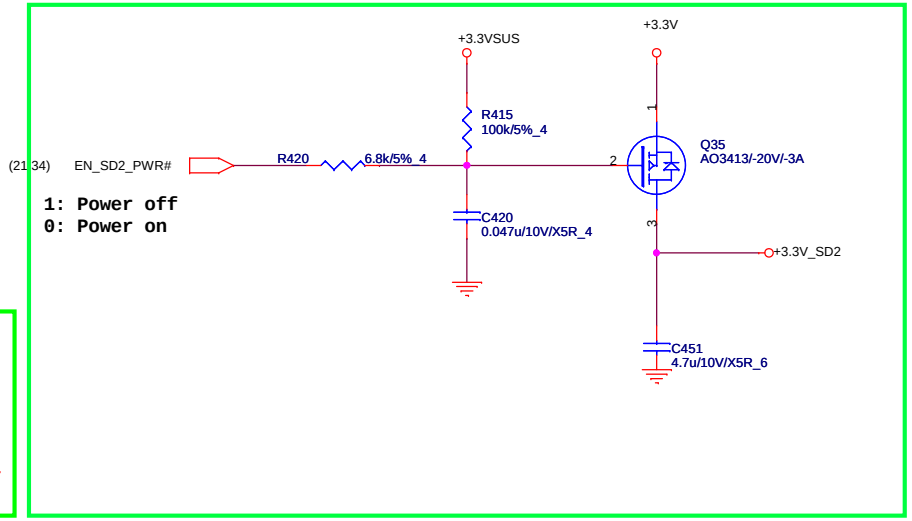
Ext. SD2 PULLUP



LAYOUT:
Close to Connector with Short Stub

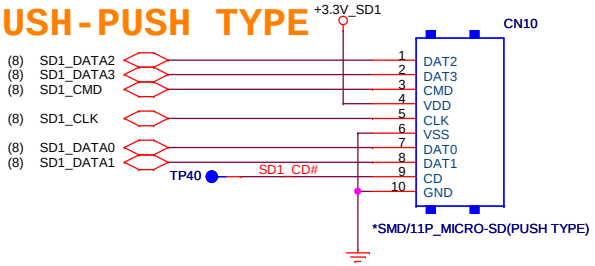






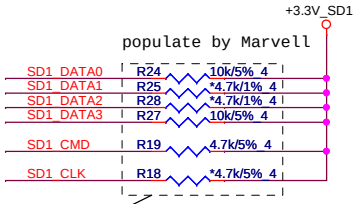
Int. SD1 Card Reader

PUSH-PUSH TYPE

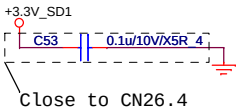


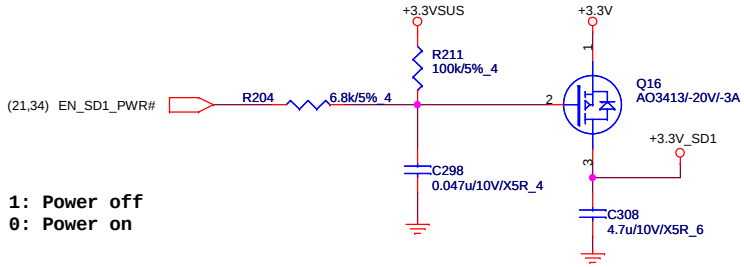
SD Write Protect Detection
(0: Write Enable; 1: Write Protect)

Int. SD1 PULLUP

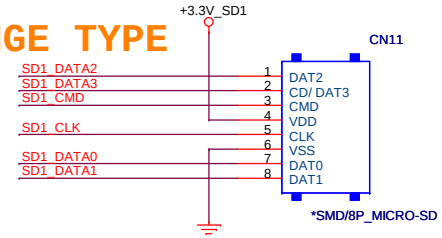


LAYOUT:
Close to Connector with Short Stub





HINGE TYPE

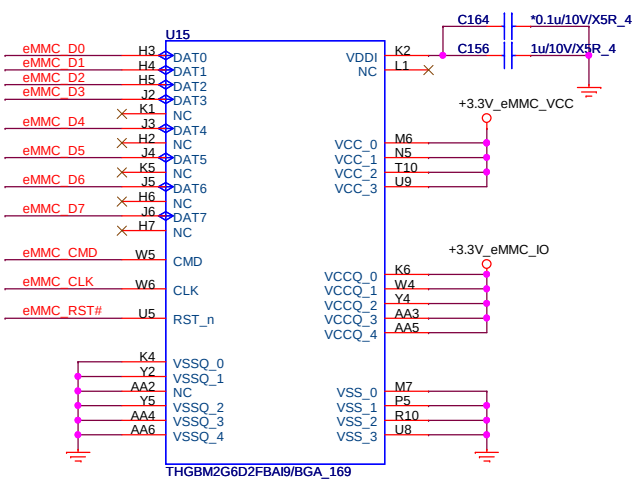


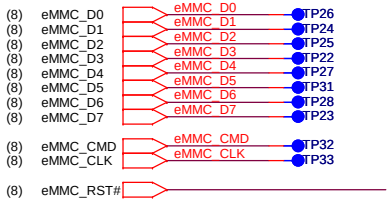
Quanta Computer Inc.
PROJECT : CL4

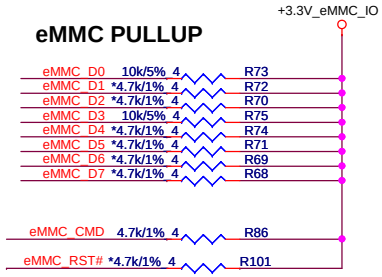
Size	Document Number	Rev
	MICRO SD & SD SLOTS	1A

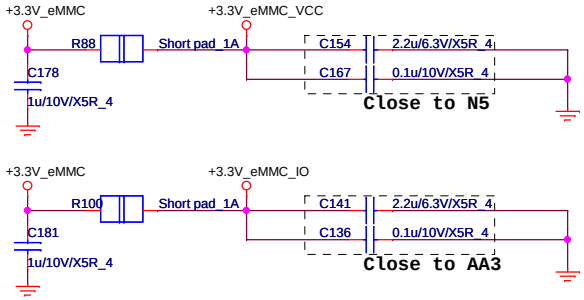
Date: Wednesday, January 30, 2013 Sheet 19 of 40

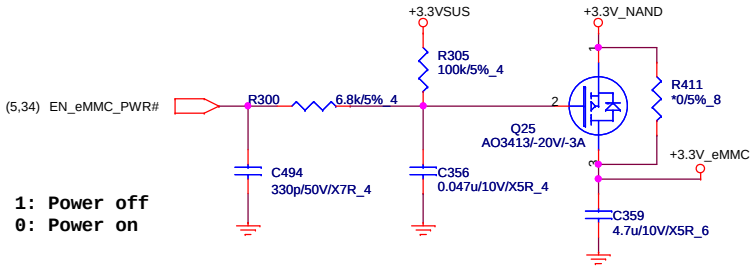
eMMC











TOS -- 8G -- AKE3QZPT000
TOS -- 16G -- AKE3RZPT000
TOS -- 32G -- AKE3SZPT001

HYU -- 8G -- AKE3QZUTW00 ???
HYU -- 16G -- AKE3RZUTW00
HYU -- 32G -- AKE3SZUTW00

SAM -- 8G -- AKE3QZPT503
SAM -- 16G -- AKE3RZPT501
SAM -- 32G -- AKE3SZPT500

Quanta Computer Inc.
PROJECT : CL4

Size	Document Number	Rev
	NAND FLASH (MLC)	1A

Date: Wednesday, January 30, 2013 Sheet 20 of 40

EC

EC_ID

EC ID0	Setting
A1	1/8*3VSUS
A2	2/8*3VSUS
B1	3/8*3VSUS
C1	4/8*3VSUS
C2	5/8*3VSUS

EC ID1	Setting
A1-C	1/8*3VSUS

EC_RST#

Restore

EC UART Debug port

REFLASH EC CODE

EC host communication

Suspend/resume function

Others

Fix ESD air discharge fail

Layout: close to U25

EC Crystal

32.768kHz/10ppm/12.5pF

REFLASH EC HEADER

*NA/HEADER 3X2 (Pitch 2.54mm)

HW strap pin

KS0=3 are HW trap, need to pull up 33k~47k ohm

Flash/debug pin

1213: only for +3.3V ext. SD

0122: Change to short pad

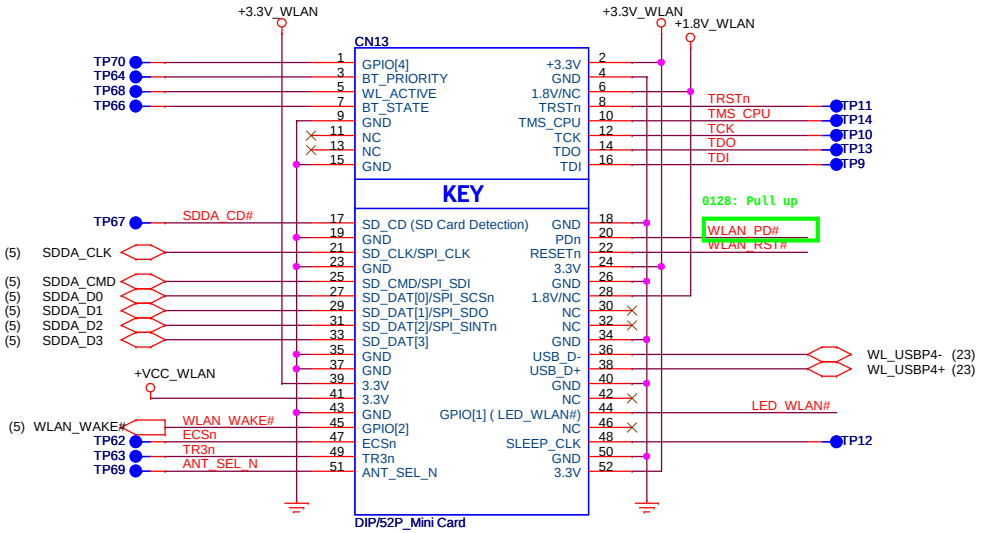
Fix SOC/EC Communications

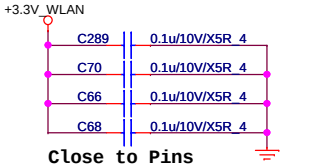
ENE's suggestion

IO3790 A1/LQFP_64P

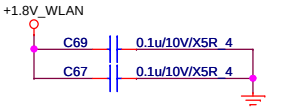
Quanta Computer Inc.	
PROJECT : CL4	
Size	Document Number: EC IO3731 — Rev: 1A
Date: Wednesday, January 30, 2013	Sheet 21 of 40

WLAN Module in Mini-PCIE Socket
Only for SDIO & USB Devices

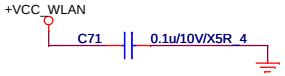




Close to Pins
(2,24,39,28) respectively

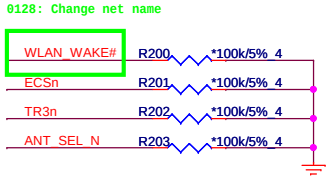


Close to
Pins (6,28) respectively



Close to Pins
(41) respectively

GPIO[4]:
WLAN MAC wake-up input/interrupt input

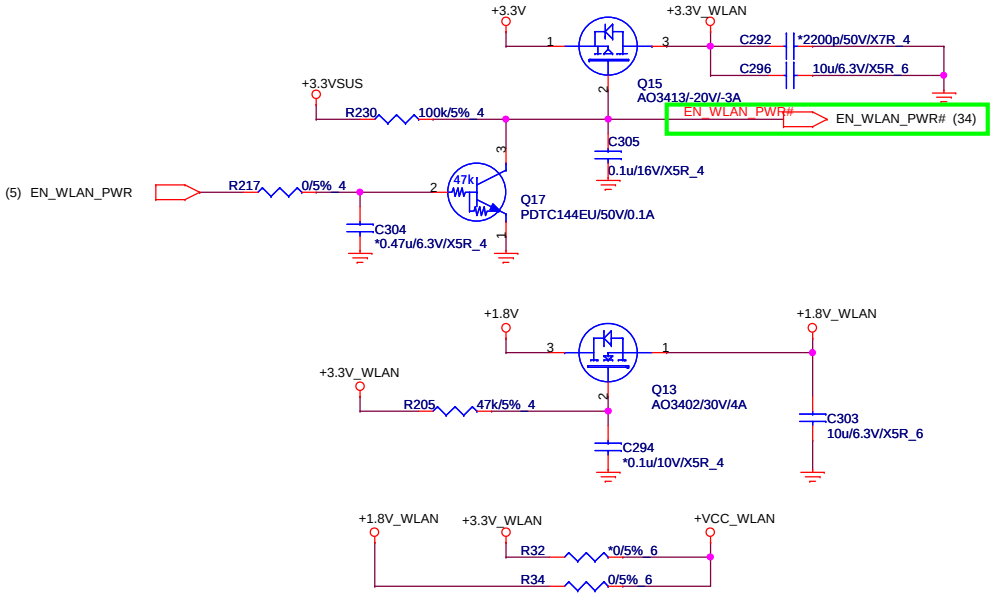


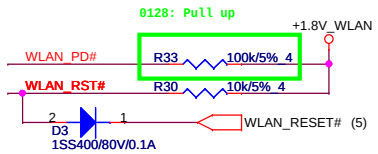
WL_GPIO[2] boot-up configuration:
0: JTAG mode enabled (pulled low by 100kohms)
1 and floating: JTAG mode disabled (Default)

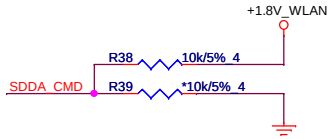
[ANT_SEL_N, TR3n] boot-up configuration:
00: General SPI (pulled-low by 100kohms)
11: SDIO (floating is OK)

ECSn boot-up configuration:
0: Boot up from SPI EEPROM (pulled-low by 100kohms)
1 & floating: Boot up from host interface (Default)

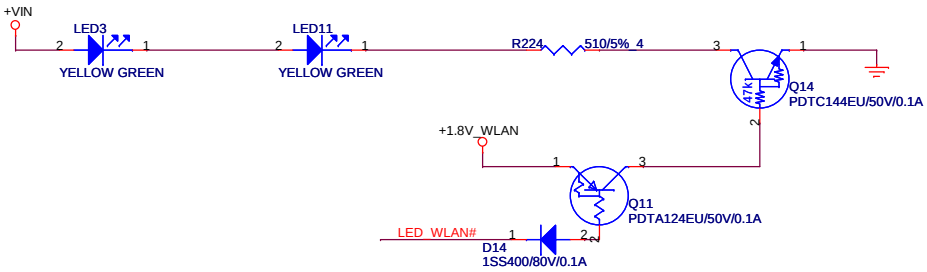
WLAN Power







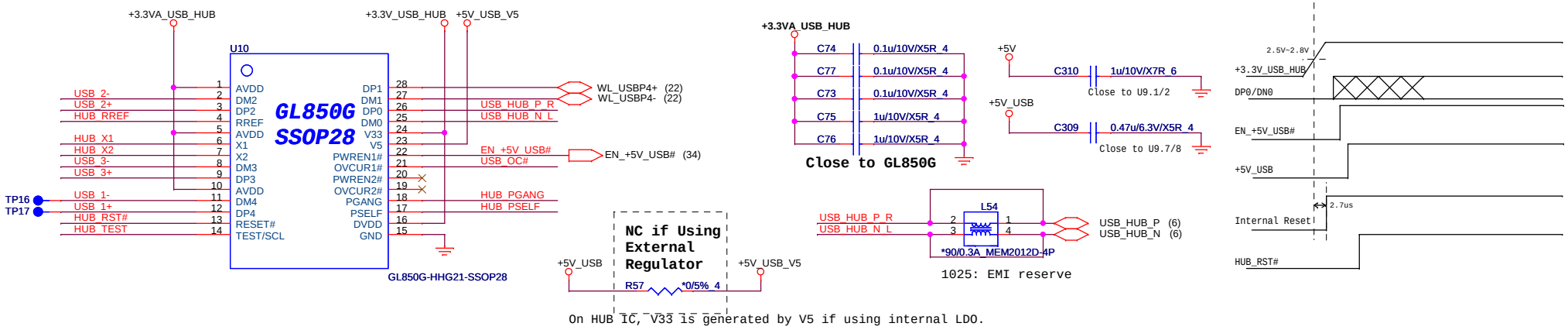
WLAN LED Indicator



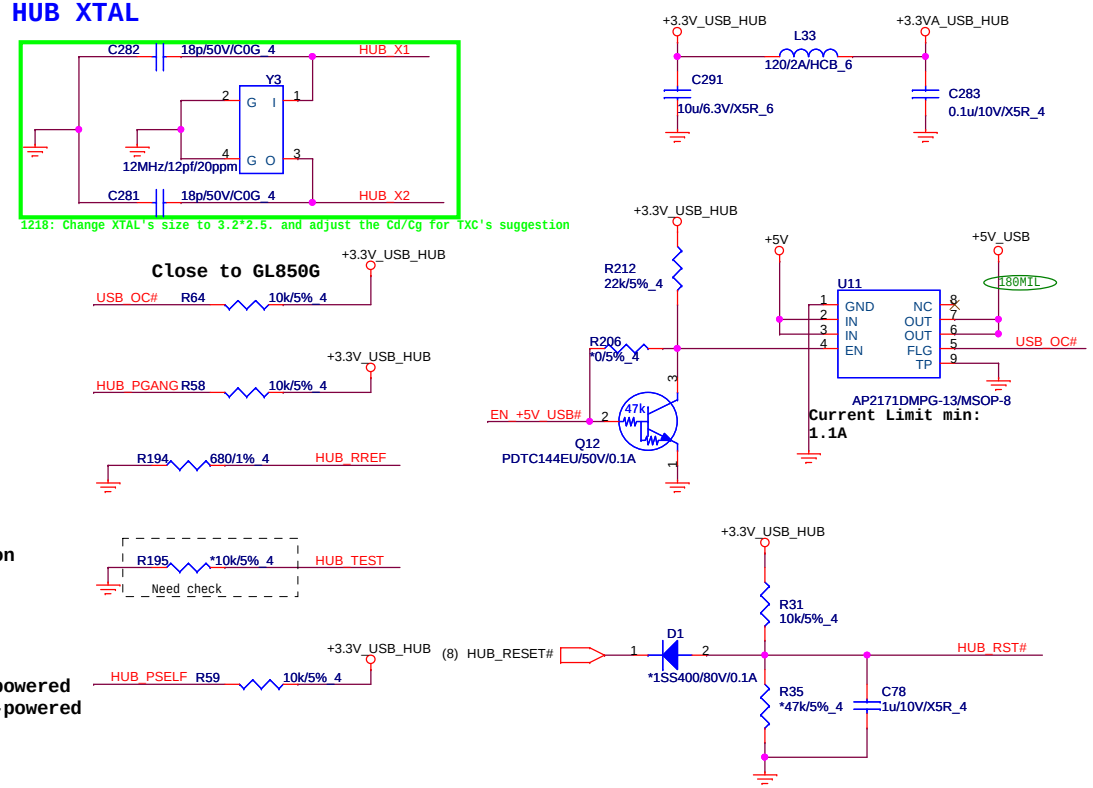
Quanta Computer Inc.		
PROJECT : CL4		
Size	Document Number: WLAN MODULE (SDIO)	Rev 1A
Date: Wednesday, January 30, 2013	Sheet 22 of 40	

USB HUB

GL850G-22 Not Support Power Switch



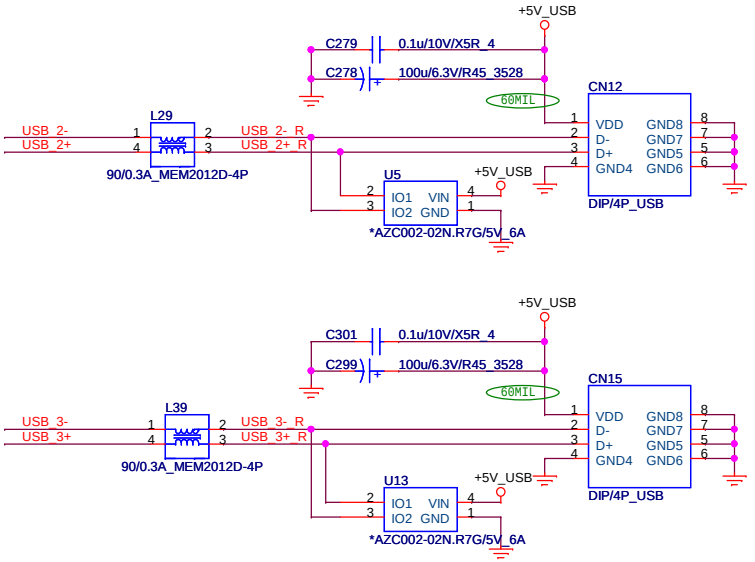
USB HUB XTAL



HUB_TEST
0: Normal Operation (Internal PD)
1: Test Mode

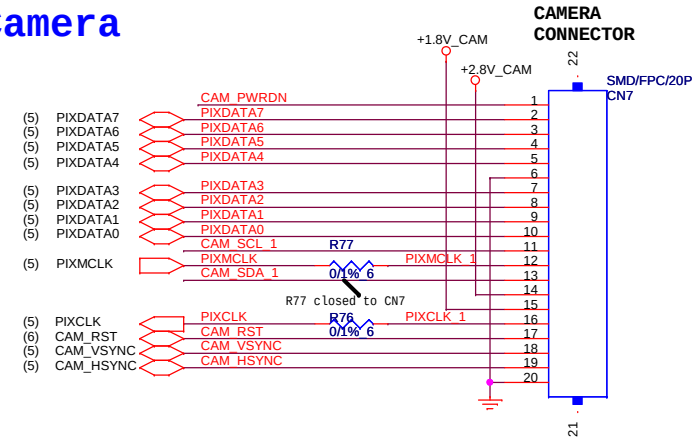
HUB_PSELF
0: GL850G is bus-powered
1: GL850G is self-powered

USB PORTS

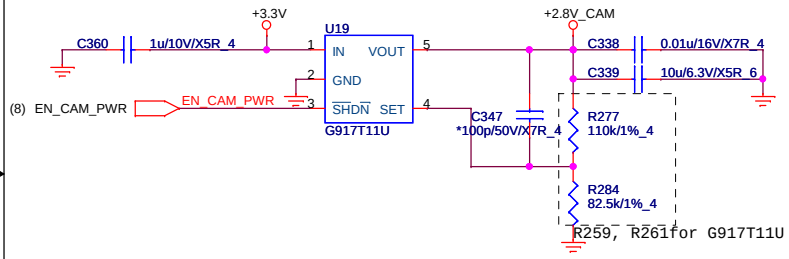


Quanta Computer Inc.		
PROJECT : CL4		
Size	Document Number	Rev
	USB HUB & PORTS	1A
Date: Wednesday, January 30, 2013	Sheet 23 of 40	

Camera

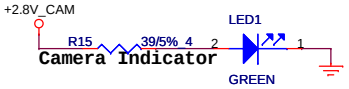


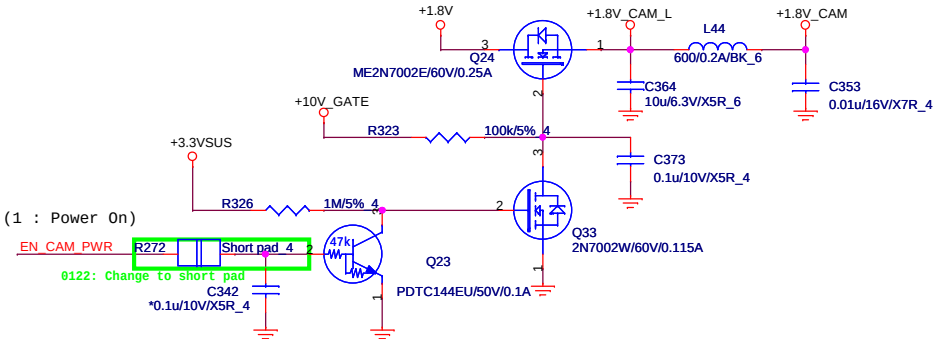
No.	Signal
1	PWDN
2	D7
3	D6
4	D5
5	D4
6	DGND
7	D3
8	D2
9	D1
10	D0
11	I2C Clock
12	MXCK(XCLK)
13	I2C Data
14	DOVDD
15	DVDD
16	PIXCLK
17	RESET
18	VSYNC
19	HSYNC
20	AGND

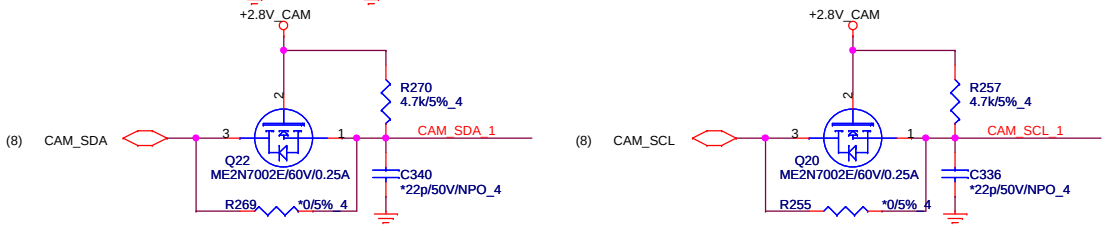


CAM_PWRDN
0: Normal mode
1: Power down mode

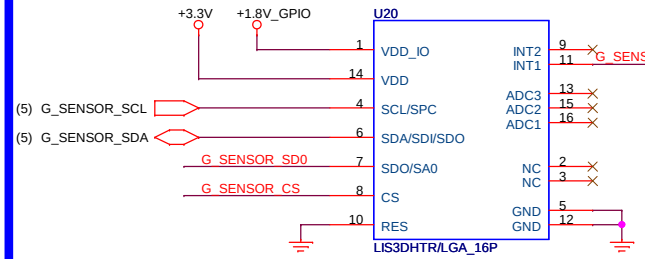
CAM_RST
0: Reset mode
1: Normal mode



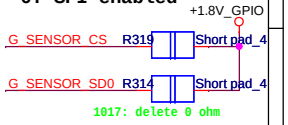


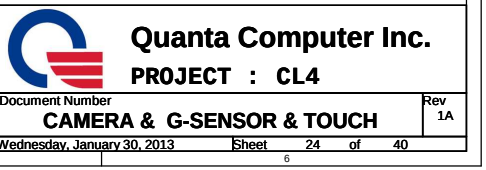


Accelerometer (Default)

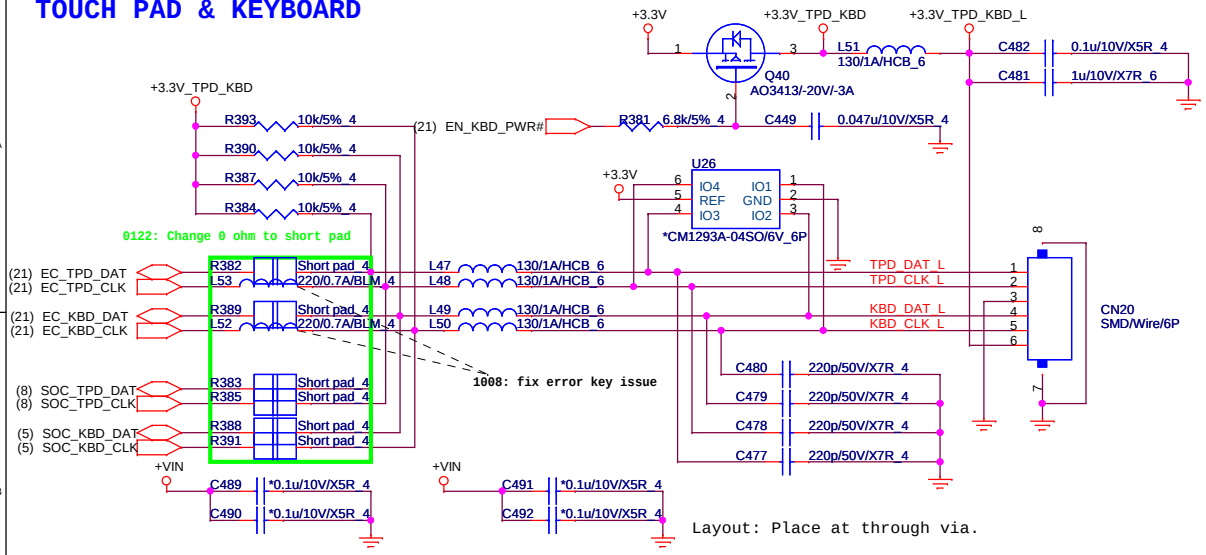


G_SENSOR_CS
1: I2C mode
0: SPI enabled

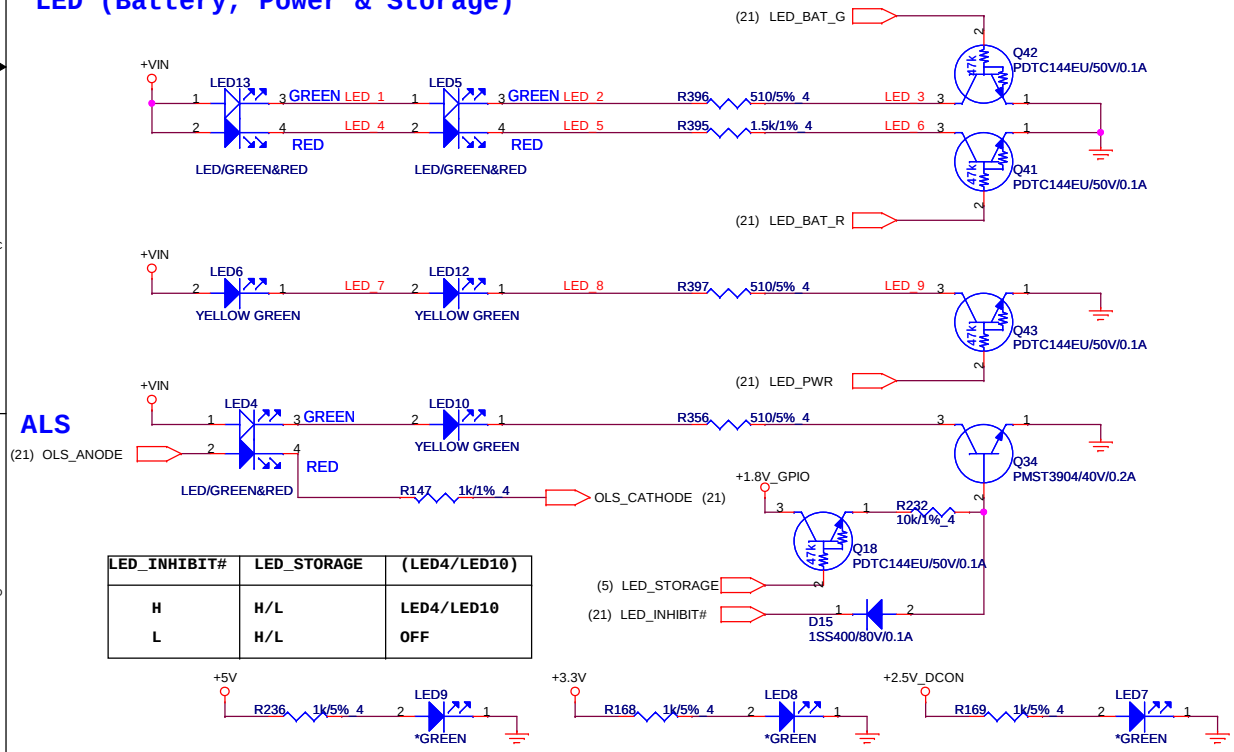




TOUCH PAD & KEYBOARD



LED (Battery, Power & Storage)

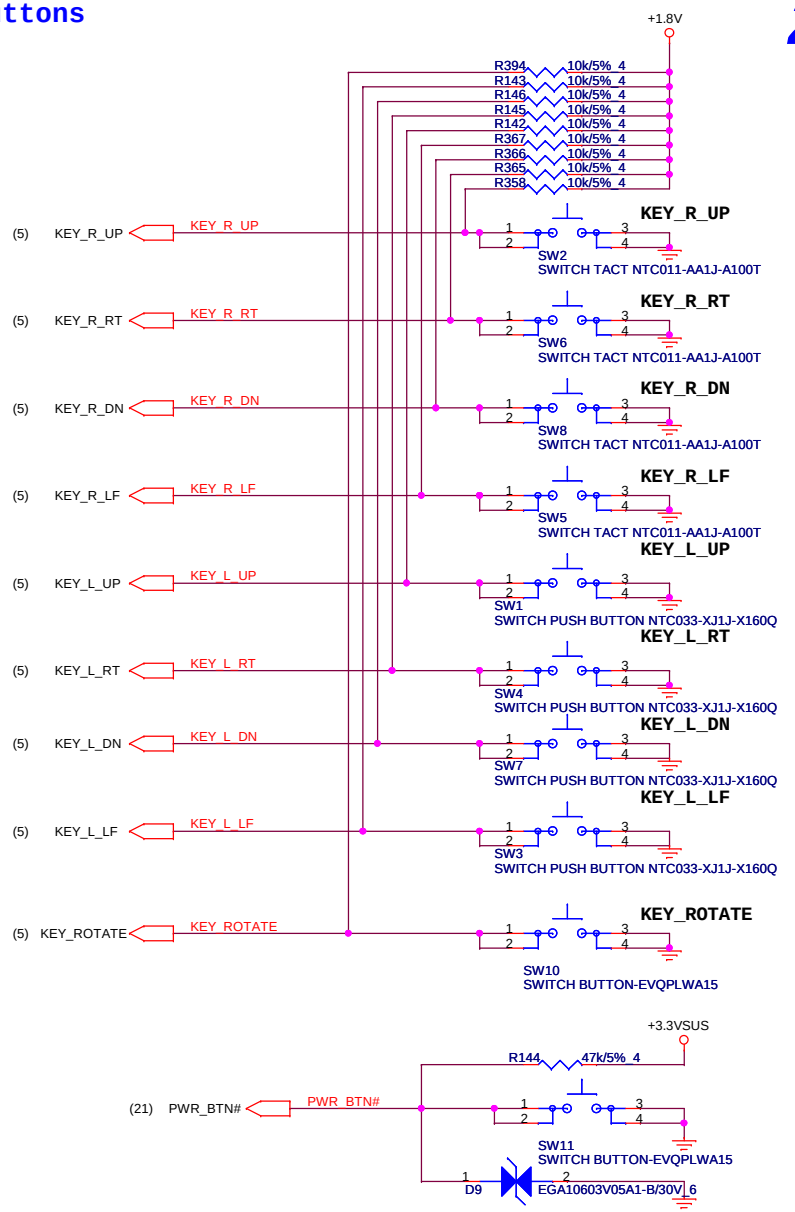


ALS

(21) OLS_ANODE

LED_INHIBIT#	LED_STORAGE	(LED4/LED10)
H	H/L	LED4/LED10
L	H/L	OFF

Buttons

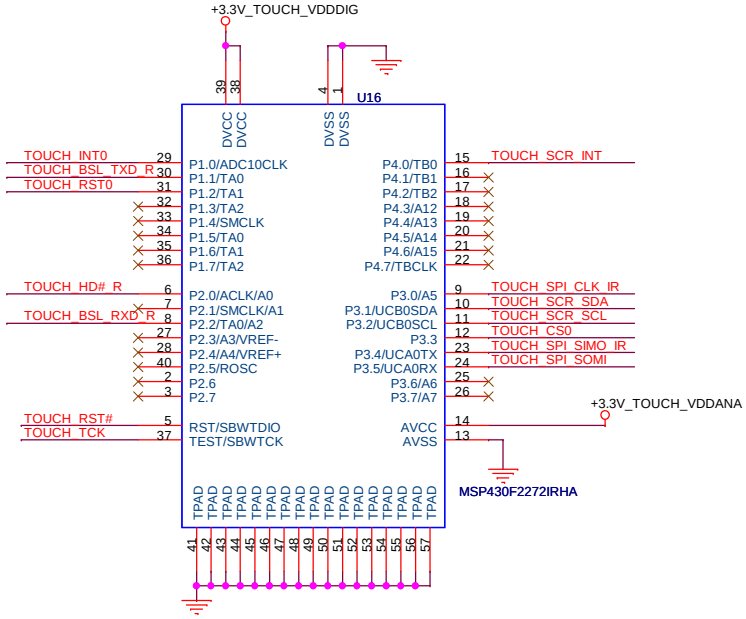


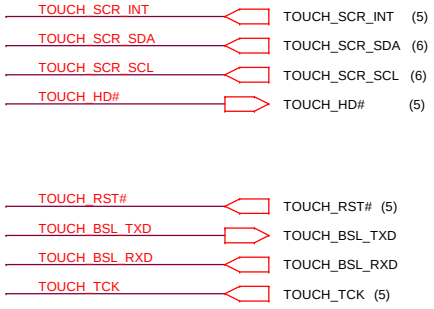
Quanta Computer Inc.

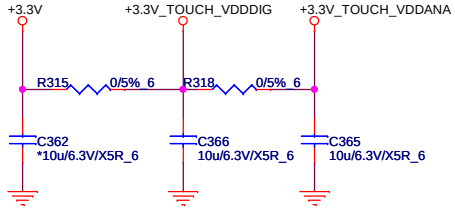
PROJECT : CL4

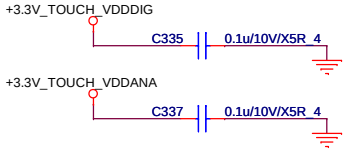
Size	Document Number	Rev
	TPD/KBD/LED/MR SENSOR/BUTTON	1A

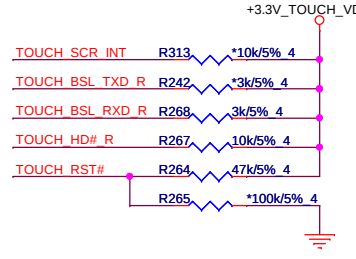
Date: Wednesday, January 30, 2013 Sheet 25 of 40

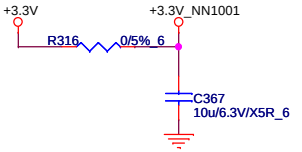


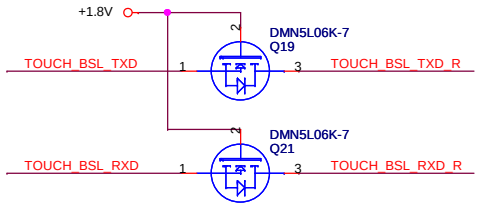


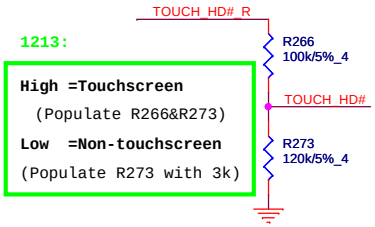


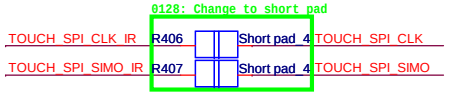


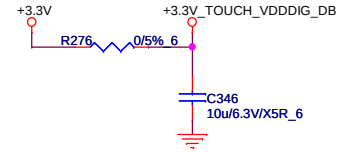


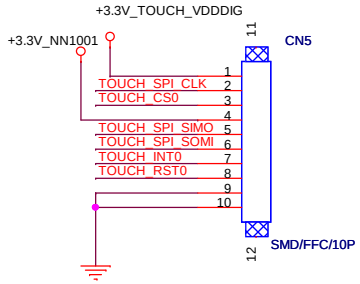


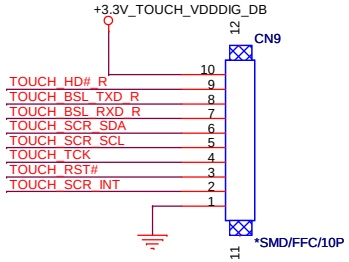












Quanta Computer Inc.

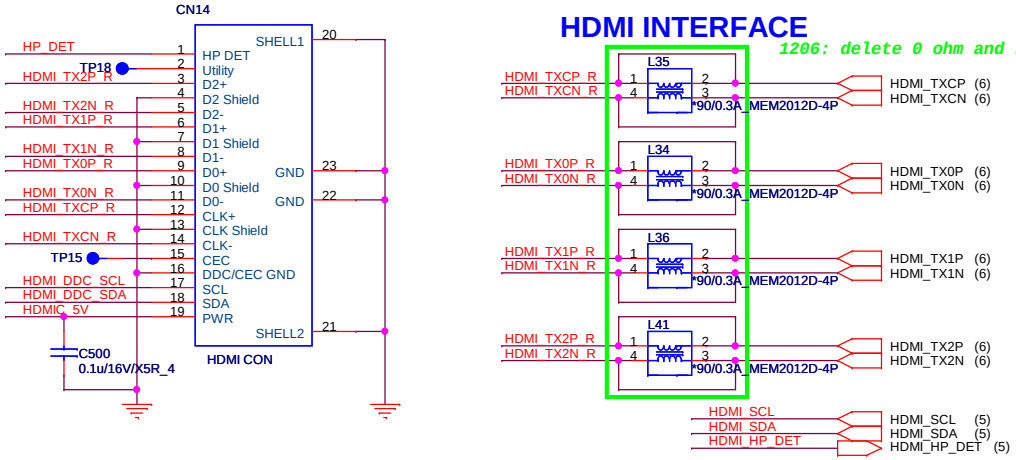
PROJECT : CL4

Size	Document Number	Rev
	NEONODE	1A

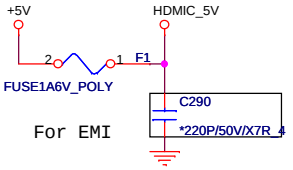
Date: Wednesday, January 30, 2013 Sheet 26 of 40

HDMI INTERFACE

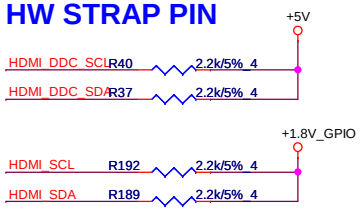
1206: delete 0 ohm and reserve common choke



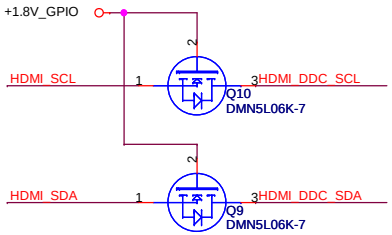
HDMI POWER SUPPLY



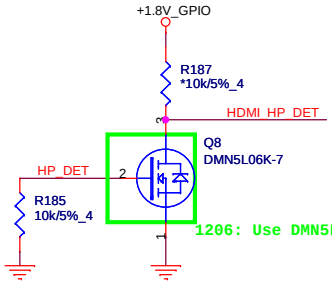
HW STRAP PIN



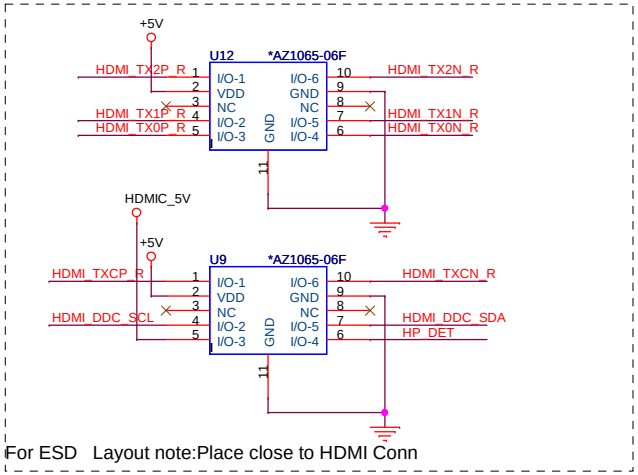
I2S BUS LEVEL SHIFT



HDMI HOT PLUG

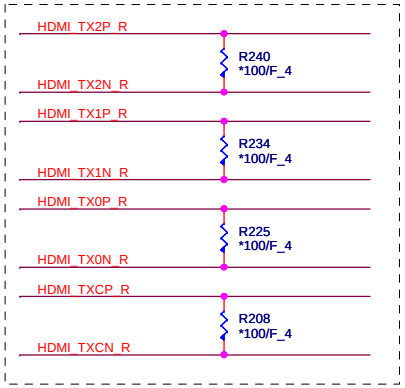


1206: Use DMN5L06k-7 with ESD protection.



For ESD Layout note:Place close to HDMI Conn

EMI reserve for HDMI

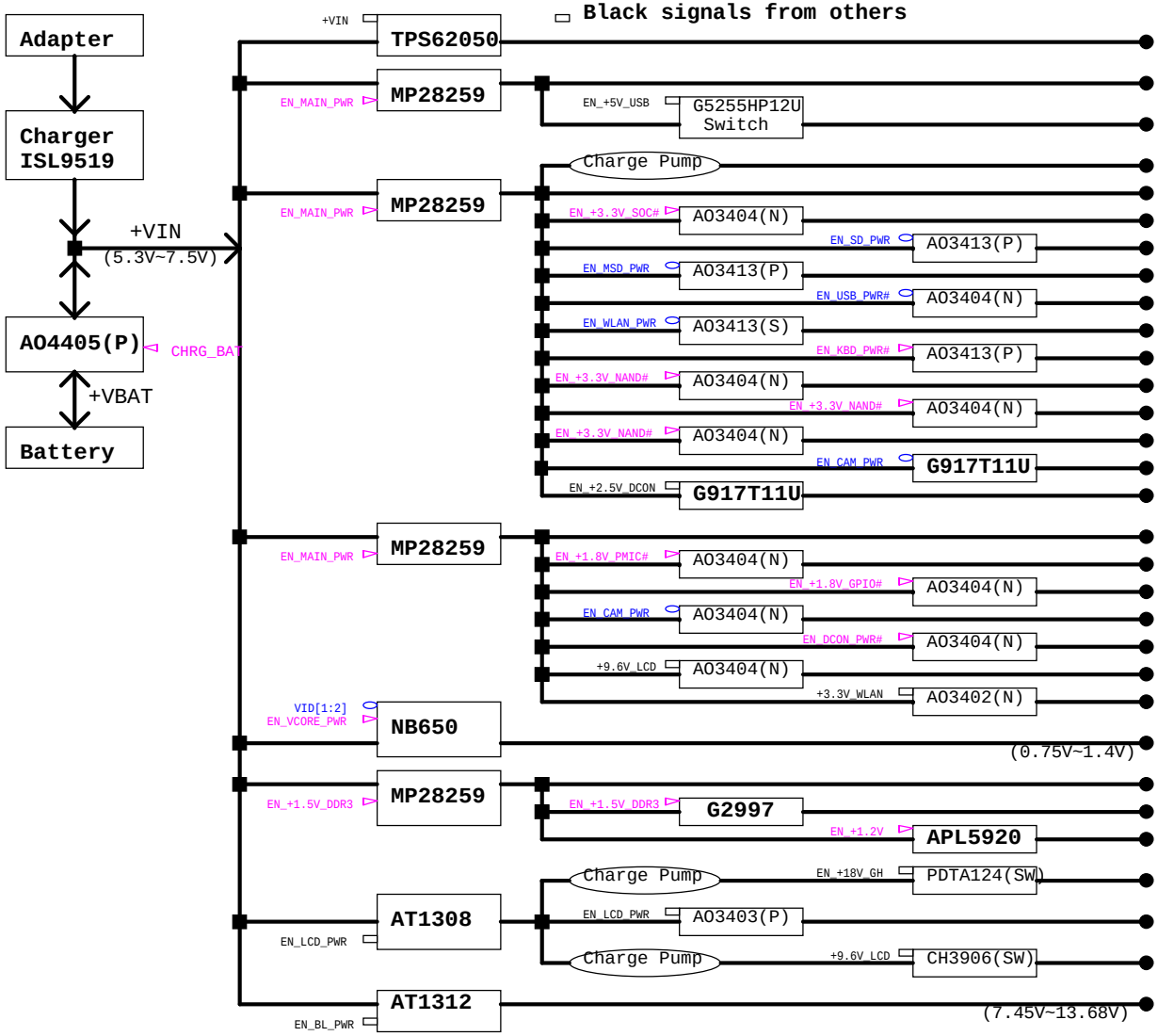


Quanta Computer Inc.
PROJECT : CL4

Size	Document Number	Rev
	NAND FLASH (MLC)	1A

Date: Wednesday, January 30, 2013 Sheet 27 of 40

Pink signals from EC
Blue signals from SOC
Black signals from others

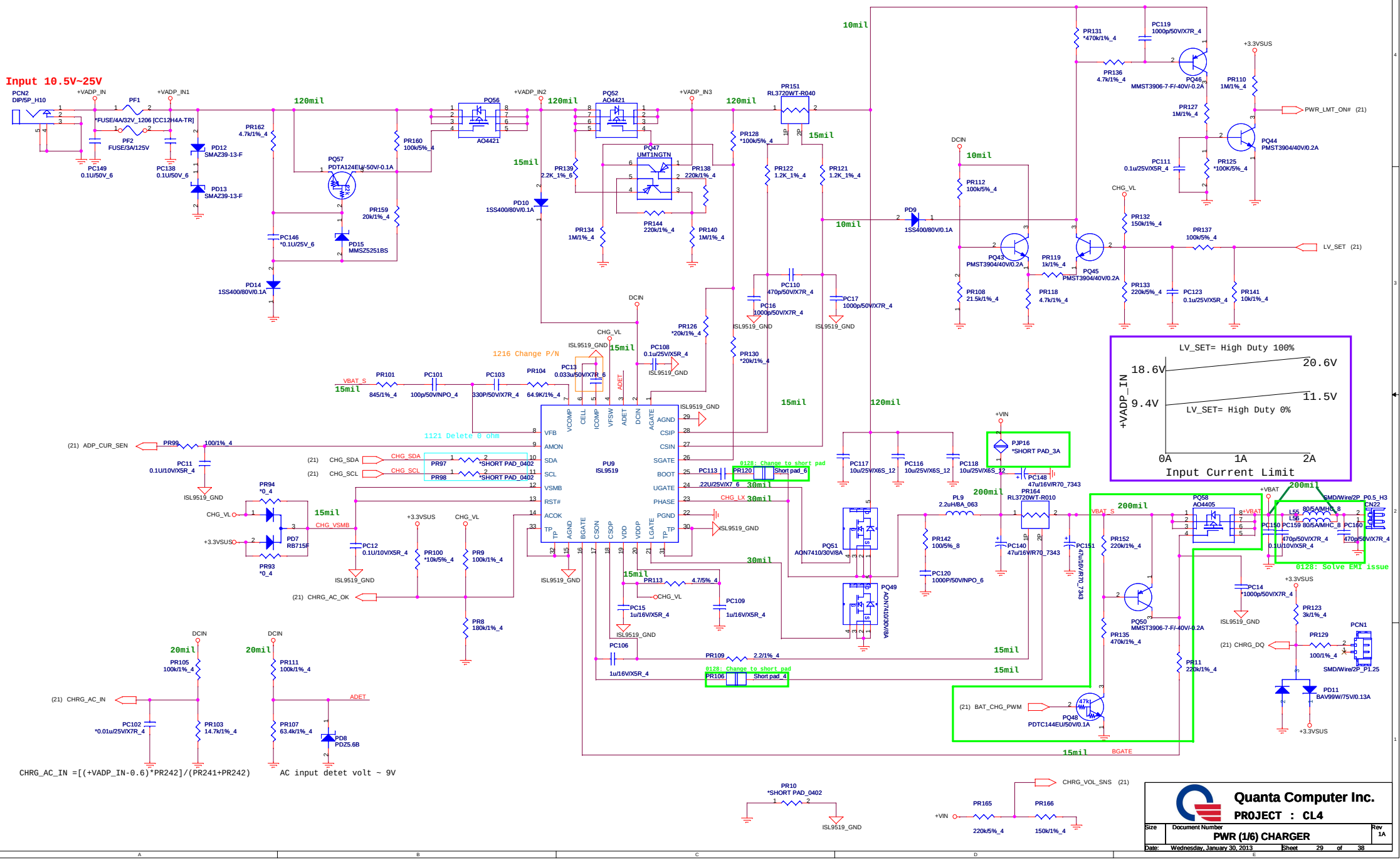


Power Rails	Rating	Succeed Power Rails
+3.3VSUS	(0.1A)	+3.3VSUS_EC, +3.3VSUSA_EC, +3.3VSUS_EC_SPI
+5V	(1.5A)	
+5V_USB		+5V_SOC_USB, +5V_USB_V5
+10V_GATE	(0.1A)	
+3.3V	(1.7A)	+3.3V_DCON, +3.3VA_AUDIO, +3.3V_SPI
+3.3V_SOC		+3.3V_SOC_HDMI, +3.3V_SOC_GPIO2, +3.3V_SOC_GPIO3, +3.3V_SOC_TWSI4
+3.3V_SD		+3.3V_SOC_SD
+3.3V_MSD		
+3.3V_USB_HUB		+3.3V_SOC_USB, +3.3VA_USB_HUB
+3.3V_WLAN		
+3.3V_TPD_KBD		
+3.3V_NAND		+3.3V_ND, +3.3V_SOC_NAND
+3.3V_BB		+3.3V_SOC_BB
+3.3V_USIM		+3.3V_SOC_USIM
+2.8V_CAM	(60mA)	
+2.5V_DCON	(0.1A)	+2.5V_DCON_IN,
+1.8V	(1.0A)	+1.8V_SOC_PLLM, +1.8V_SOC_HDMI, +1.8V_AUDIO,
+1.8V_PMIC		+1.8V_SOC_PMIC(1, 2), +1.8V_SOC_SBUS
+1.8V_GPIO		+1.8V_SOC_GPIO1
+1.8V_CAM		
+1.8V_DCON		+1.8V_DCON_(PIN7, PIN39, 97)
+1.8V_LCD		+1.8V_LCD_IN,
+1.8V_WLAN		
+VCORE	(3.5A)	
+1.5V_DDR3	(1.65A)	
+0.75VTERM_DDR3	(0.36A)	
+1.2V	(0.1A)	+1.2V_SOC_CSI, +1.2V_SOC_DSI, +1.2V_SOC_HSIC1
+18V_GH	(20mA)	
+9.6V_LCD	(50mA)	
-7V_GL	(12mA)	
+VCC_LED	(60mA)	

Quanta Computer Inc.
PROJECT : CL4

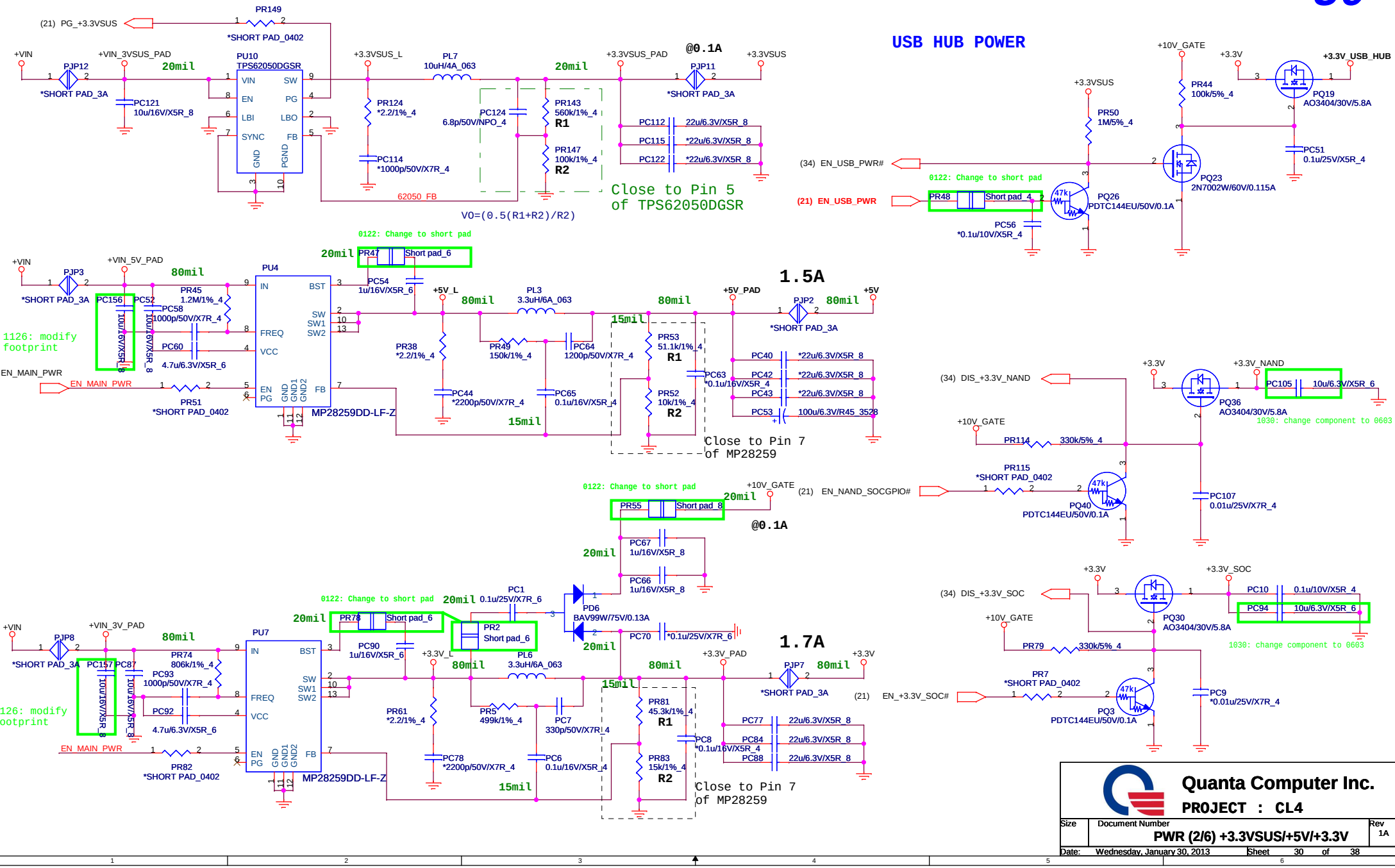
Size	Document Number	Rev
	POWER MAP	1A

Date: Wednesday, January 30, 2013 Sheet 28 of 38

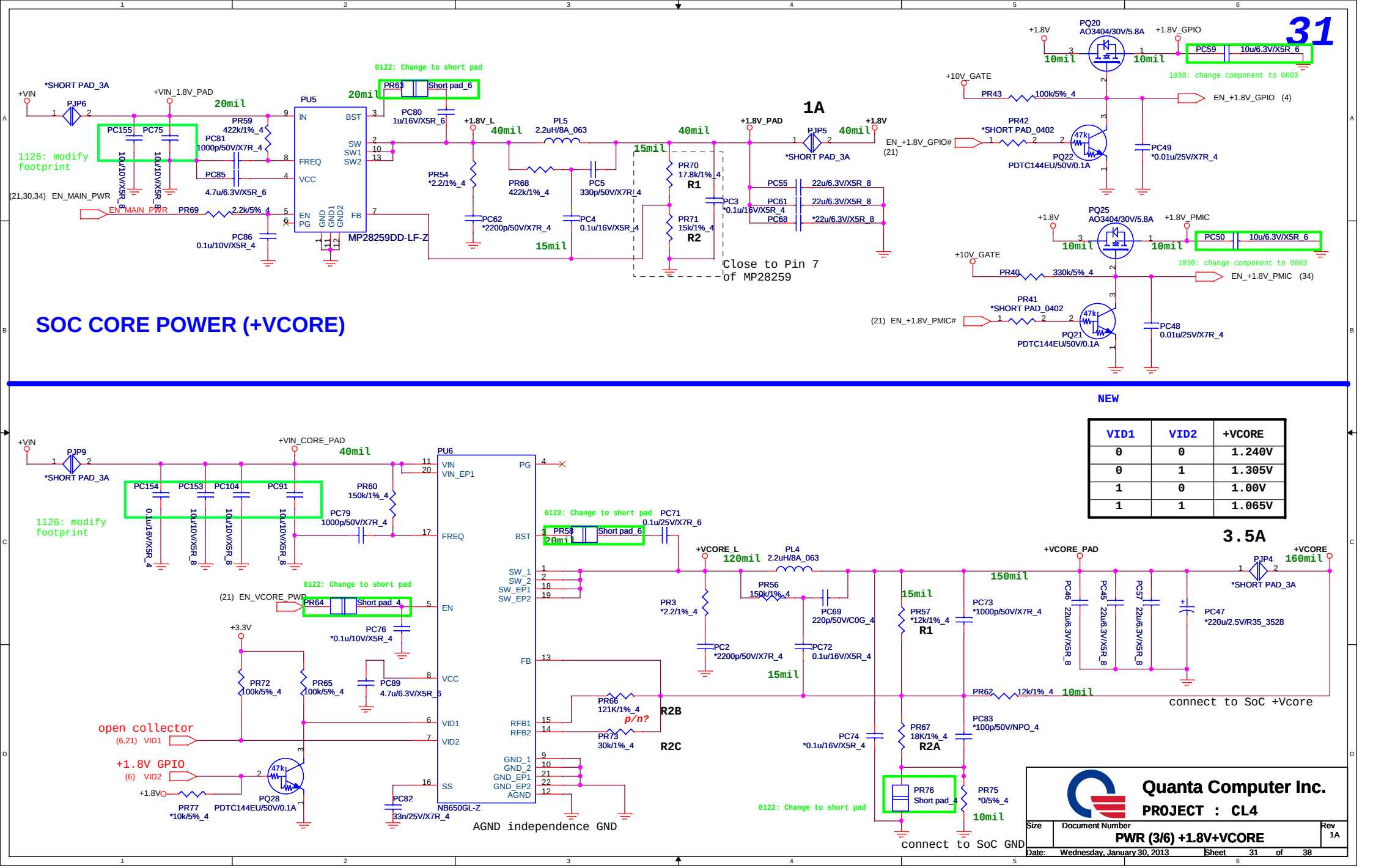


Quanta Computer Inc.			
PROJECT : CL4			
Size	Document Number		Rev
	PWR (1/6) CHARGER		1A
Date: Wednesday, January 30, 2013	Sheet 29 of 38		

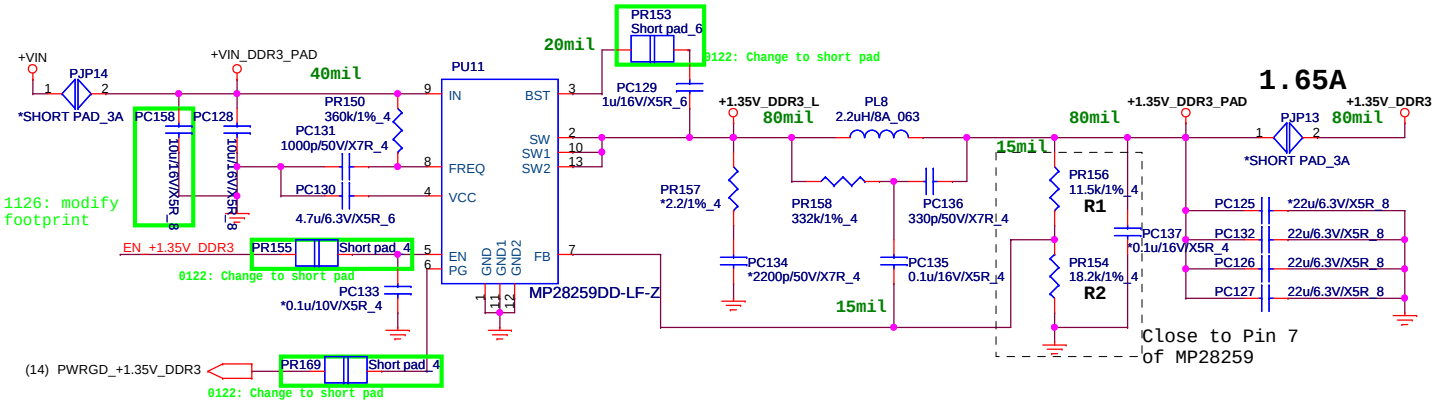
USB HUB POWER

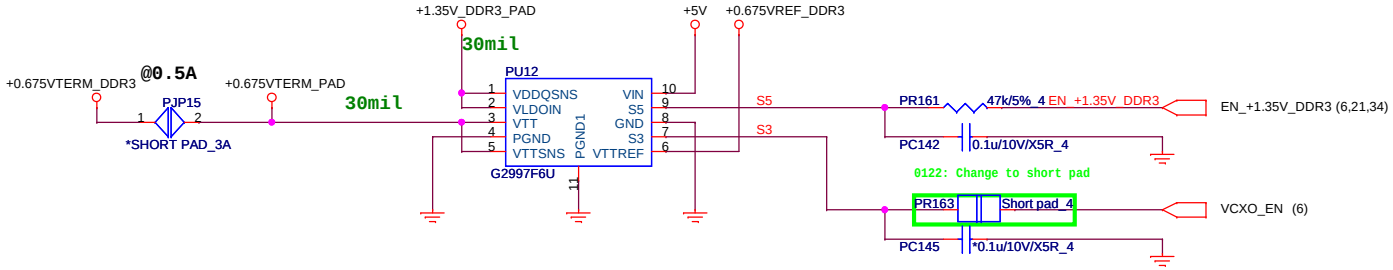


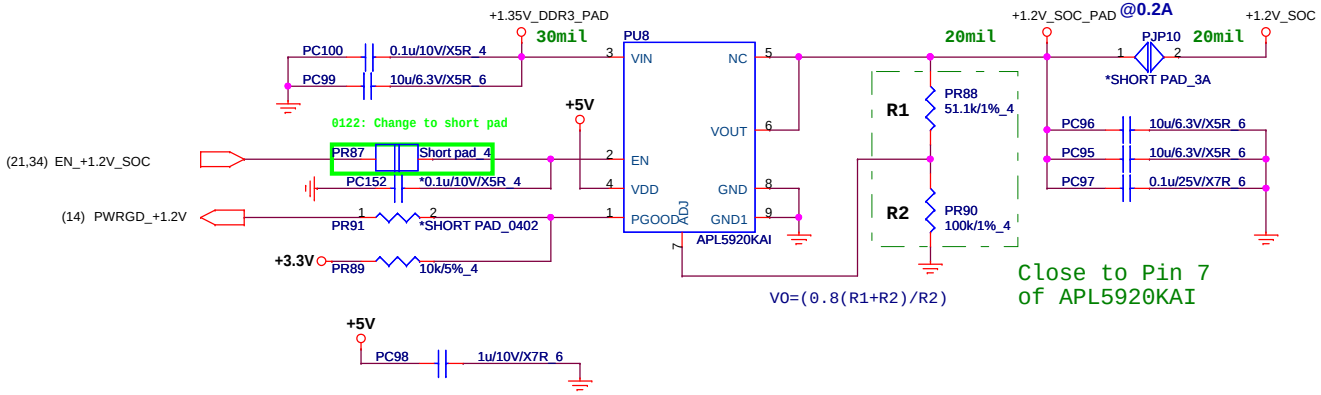
Quanta Computer Inc.		
PROJECT : CL4		
Size	Document Number	Rev
	PWR (2/6) +3.3VSUS/+5V/+3.3V	1A
Date: Wednesday, January 30, 2013	Sheet 30 of 38	


31
SOC CORE POWER (+VCORE)
1A
MP28259DD-LF-Z
Close to Pin 7 of MP28259
1126: modify footprint
0122: Change to short pad
1030: change component to 0603
NEW
VID1 VID2 +VCORE
0 0 1.240V
0 1 1.305V
1 0 1.00V
1 1 1.065V
3.5A
NB650GL-Z
AGND independence GND
connect to SoC +Vcore
connect to SoC GND
Quanta Computer Inc.
PROJECT : CL4
PWR (3/6) +1.8V+VCORE
Size
Document Number
Rev 1A
Date: Wednesday, January 30, 2013
Sheet 31 of 38

DDR3 POWER

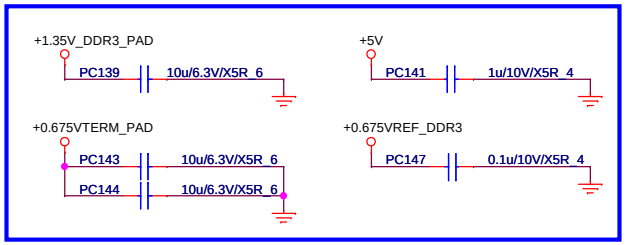




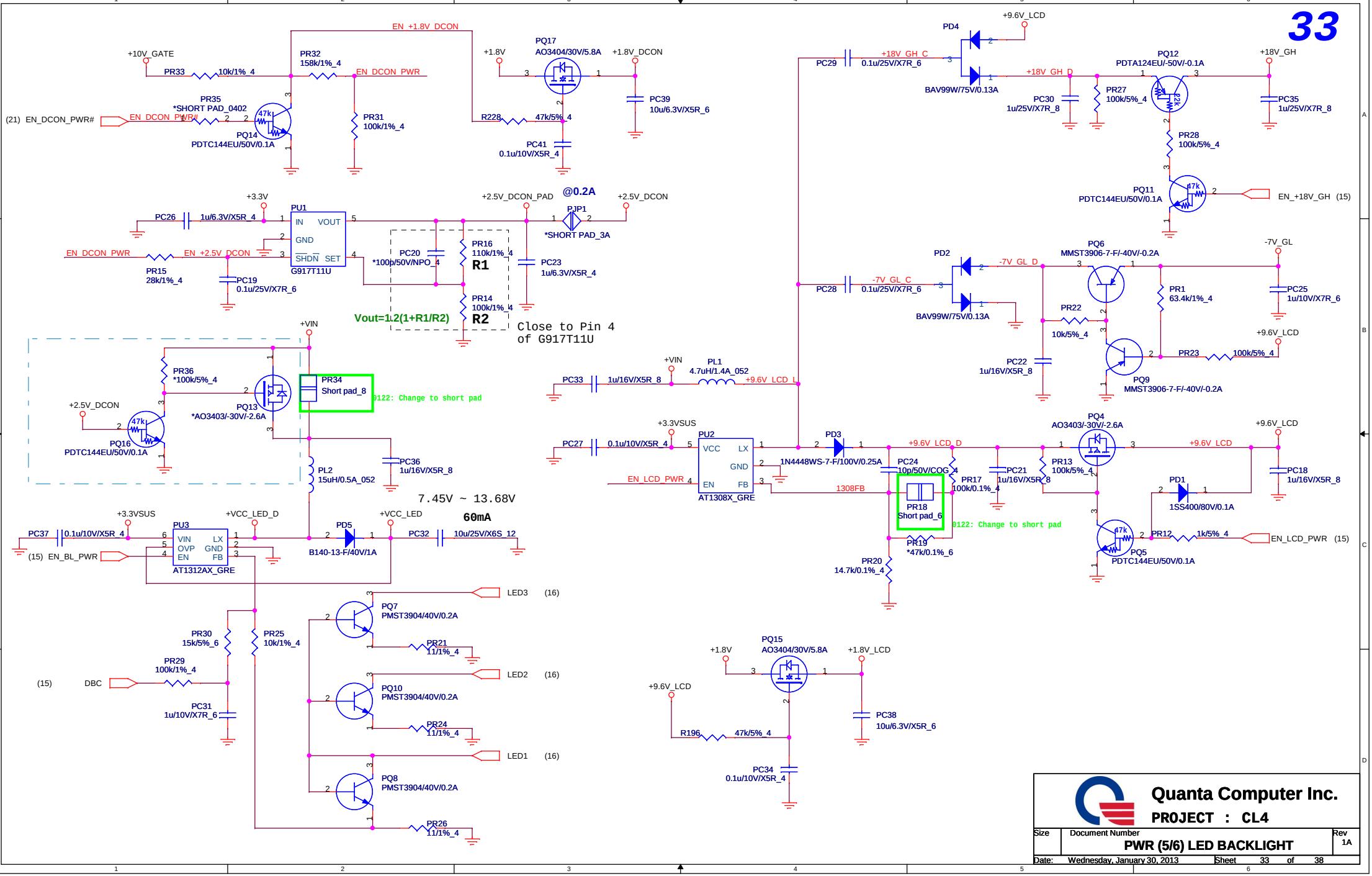


	PR46	PR47	Voltage
DDR3	15k	18.2k	1.5V
DDR3L	11.5k	18.2k	1.35V

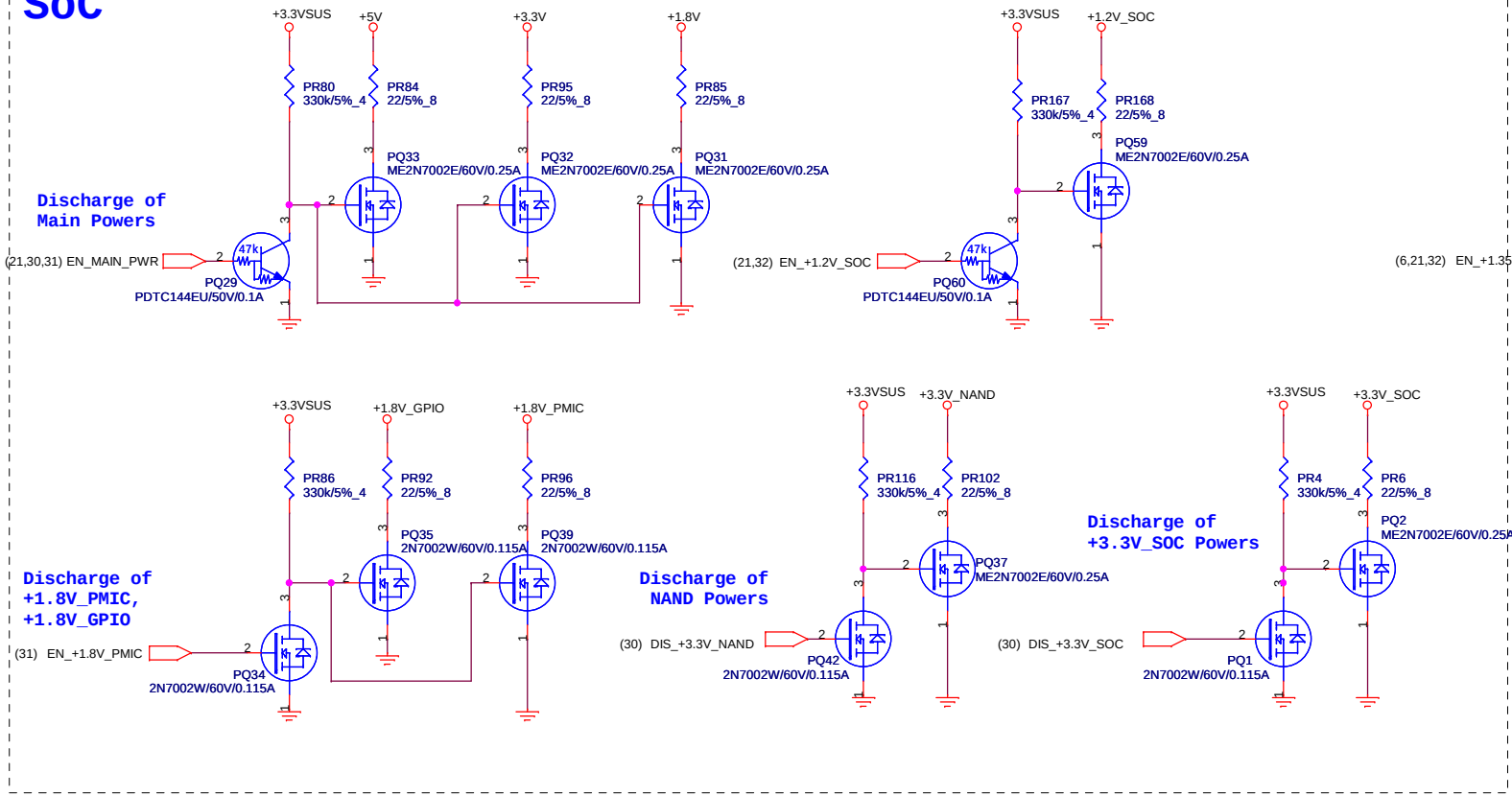
To Near PU18 PIN



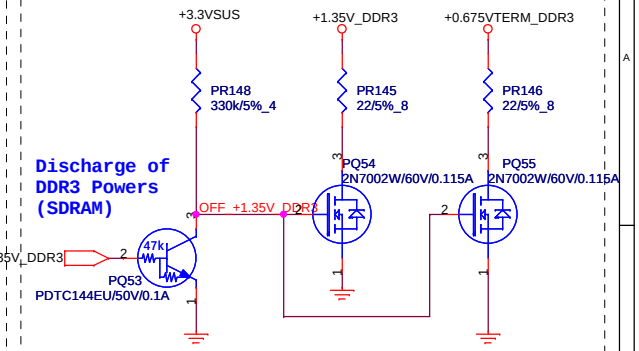
Quanta Computer Inc.	PROJECT : CL4	
Size	Document Number: PWR (4/6) DDR3 PWR/+1.2V	Rev: 1A
Date: Wednesday, January 30, 2013	Sheet 32 of 38	


33
+10V_GATE
PR33 10k/1%_4
PR32 158k/1%_4
EN_+1.8V_DCON
EN_DCON_PWR
PR35 *SHORT PAD_0402
(21) EN_DCON_PWR#
EN_DCON_PWR#
PQ14 PDTC144EU/50V/0.1A
PR31 100k/1%_4
+1.8V
PQ17 AO3404/30V/5.8A
+1.8V_DCON
PC39 10u/6.3V/X5R_6
R228 47k/5%_4
PC41 0.1u/10V/X5R_4
+3.3V
PU1
PC26 1u/6.3V/X5R_4
IN VOUT
GND
SHDN SET
G917T11U
EN_DCON_PWR
EN_+2.5V_DCON
PR15 28k/1%_4
PC19 0.1u/25V/X7R_6
PC20 *100p/50V/NPO_4
PR16 110k/1%_4
R1
PR14 100k/1%_4
R2
Vout=1.2(1+R1/R2)
+2.5V_DCON_PAD
@0.2A
PJP1
*SHORT PAD_3A
+2.5V_DCON
PC23 1u/6.3V/X5R_4
Close to Pin 4 of G917T11U
+VIN
PR36 *100k/5%_4
PQ13 *AO3403/-30V/-2.6A
PR34 Short pad_8
0122: Change to short pad
+2.5V_DCON
PQ16 PDTC144EU/50V/0.1A
PL2 15uH/0.5A_052
PC36 1u/16V/X5R_8
7.45V ~ 13.68V
60mA
+3.3VSUS
PU3
PC37 0.1u/10V/X5R_4
VIN LX
OVP GND
EN FB
AT1312AX_GRE
(15) EN_BL_PWR
+VCC_LED_D
PD5
B140-13-F/40V/1A
+VCC_LED
PC32 10u/25V/X6S_12
PR30 15k/5%_6
PR25 10k/1%_4
PR29 100k/1%_4
(15) DBC
PC31 1u/10V/X7R_6
PQ7 PMST3904/40V/0.2A
PR21 11/1%_4
LED3 (16)
PQ10 PMST3904/40V/0.2A
PR24 11/1%_4
LED2 (16)
PQ8 PMST3904/40V/0.2A
PR26 11/1%_4
LED1 (16)
+VIN
PL1 4.7uH/1.4A_052
PC33 1u/16V/X5R_8
+9.6V_LCD_L
+3.3VSUS
PC27 0.1u/10V/X5R_4
PU2
VCC LX
GND
EN FB
AT1308X_GRE
EN_LCD_PWR
PD3
1N4448WS-7-F/100V/0.25A
+9.6V_LCD_D
1308FB
PC24 10p/50V/COG_4
PR18 Short pad_6
PR17 100k/0.1%_4
PR19 *47k/0.1%_6
PR20 14.7k/0.1%_4
0122: Change to short pad
PC21 1u/16V/X5R_8
PR13 100k/5%_4
PQ4 AO3403/-30V/-2.6A
+9.6V_LCD
PC18 1u/16V/X5R_8
PD1 1SS400/80V/0.1A
PR12 1k/5%_4
EN_LCD_PWR (15)
PQ5 PDTC144EU/50V/0.1A
+1.8V
PQ15 AO3404/30V/5.8A
+1.8V_LCD
+9.6V_LCD
R196 47k/5%_4
PC38 10u/6.3V/X5R_6
PC34 0.1u/10V/X5R_4
+9.6V_LCD
PD4 BAV99W/75V/0.13A
+18V_GH_C
PC29 0.1u/25V/X7R_6
+18V_GH_D
PC30 1u/25V/X7R_8
PQ12 PDTA124EU/-50V/-0.1A
PR27 100k/5%_4
+18V_GH
PC35 1u/25V/X7R_8
PR28 100k/5%_4
PQ11 PDTC144EU/50V/0.1A
EN_+18V_GH (15)
-7V_GL
PD2 BAV99W/75V/0.13A
-7V_GL_C
PC28 0.1u/25V/X7R_6
-7V_GL_D
PQ6 MMST3906-7-F/-40V/-0.2A
PR1 63.4k/1%_4
PC25 1u/10V/X7R_6
PR22 10k/5%_4
PC22 1u/16V/X5R_8
PQ9 MMST3906-7-F/-40V/-0.2A
+9.6V_LCD
PR23 100k/5%_4
Quanta Computer Inc.
PROJECT : CL4
Size
Document Number
PWR (5/6) LED BACKLIGHT
Rev 1A
Date: Wednesday, January 30, 2013
Sheet 33 of 38

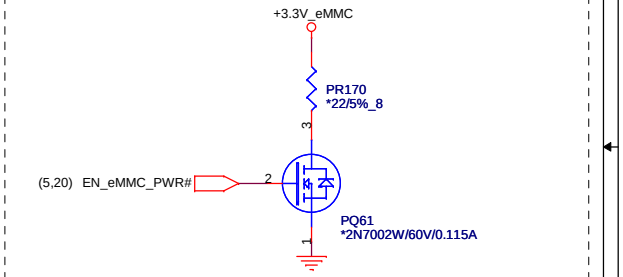
SoC



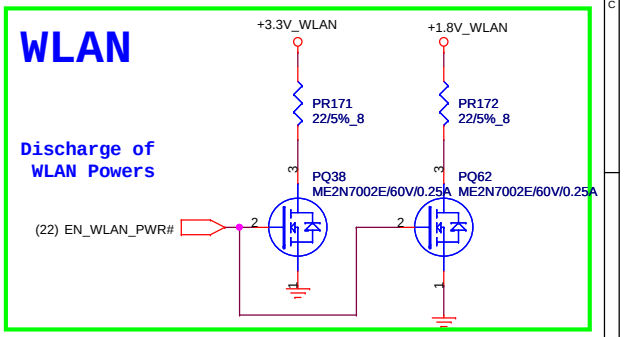
DDR3



eMMC

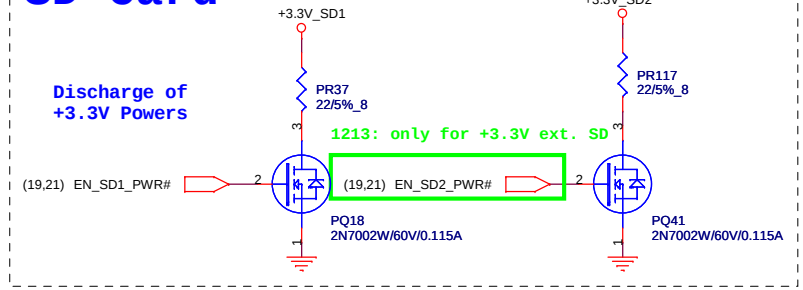


WLAN

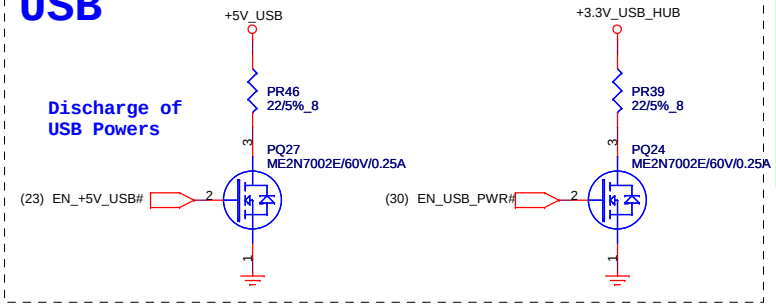


0124: Add discharge circuit to fix 8787 card disappear.

SD Card



USB



Quanta Computer Inc.
PROJECT : CL4

Size	Document Number	Rev
	DISCHARGE	1A

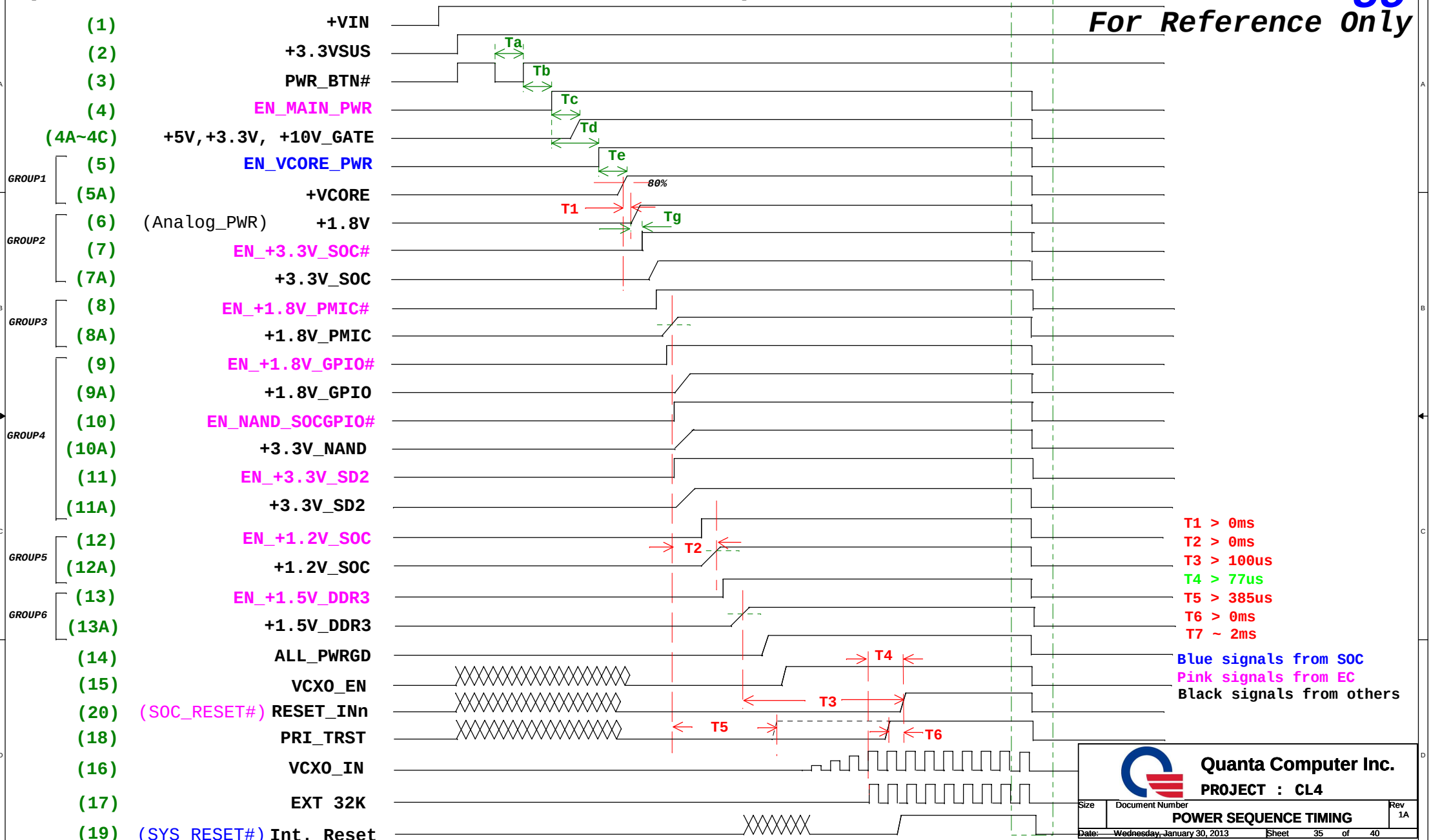
Date: Wednesday, January 30, 2013 Sheet 34 of 38

Updated on 2012/7/11

Power on sequence

OFF

For Reference Only



T1 > 0ms
T2 > 0ms
T3 > 100us
T4 > 77us
T5 > 385us
T6 > 0ms
T7 ~ 2ms

Blue signals from SOC
Pink signals from EC
Black signals from others

Quanta Computer Inc.
PROJECT : CL4

Size	Document Number	Rev
	POWER SEQUENCE TIMING	1A

Date: Wednesday, January 30, 2013 Sheet 35 of 40

Schematic modify Item and History :

A2-->B1

1.Fixing +3.3V_SOC -

1.Change PR79 to a 10K resistor

2.Fixing +3.3V_SOC -

1.PR62 (or PR57) should be 12.0K
2.PR67 should be 18.0K
3.PR66 should be 120K
4.PR73 should be 30.0K

3.Pulse JTAG Reset at start of day -

1.Add a small schottky between EN_+1.35V_DDR3 and PRI_TRST#. The cathode of the diode should be connected to EN_+1.35V_DDR3.
2.Remove the 100K resistor from R335.
3.Populate R334 with a 100K resistor

4.Fix MMP3 B0 errata 1.15 -

1.Replace R45 with a 10 ohm resistor (pref. 0603 or 0805)

5.Changing to a +1.8V SPI Flash -

1...

6.Changing to a +1.8V SPI Flash -

1.Remove the resistors from the following locations: R94 (3K), R98 (3K), R253 (3K), R258 (3K), R372 (1.2K), R373 (1.2K), and R375 (1.2K)
2.Replace D18 with a 3K resistor
3.Remove Q36, and place a 3K resistor between pins 1 and 3
4.Remove Q38, and place a 3K resistor between pins 1 and 4
5.Add a 3K pullup resistor to +3.3VSUS_EC (or +3.3VSUS) to EC_SDI_MISO (Q37, pin 3).
6.Add a 3.6K pulldown from SDI_MOSI (D18 anode) to GND
7.Add a 3.6K pulldown from SDI_CLK (Q36.1) to GND
8.Add a 3.6K pulldown from SDI_CS# (Q38.1) to GND

Schematic modify Item and History :

B1-->C1

1 Change footprint-
- 1.Change C351, C354 and C355 from 0603 to 0402
- 1.Change PC59, PC50, PC94, PC105 PC96, PC95, PC39 and PC38 from 0805to 0603

2.EMI issue-
- 1.Reserve a common choke L54 on USB_HUB_P/N
- 2.Change common choke source on both USB ports.
- 3.Add two bead (EMI FILTER MHC2012S800UBP(80,5A)) between battery connector(CN22) and P-MOS(PQ58).

3.Add C494 (330pf) to fix signal noise. Need to close R300

4.Reserve a disharge circuit on eMMC power and a pulled-up reisior R101 on eMMC_RST to fix SDHCI error.

5.Add C487 (330pf) and C488 (330pf) to fix ESD air discharge issue

6.Using +1.8V SPI Flash -
- 1.Populate U27 and remove Q36
- 2.Add R413(39 ohm)between SOC_SPI_CLK and SPI_CLK
- 3.Change R295 to 1 kohm

7.Add C485 (0.1uf) to close U7.3 for fixing power noise.

8.Change the following resistors from 0 ohm to short-
R118,R105,R101,R79,R237,R229,R263,R103,R36,R60,R303,R174, R175,R363

9.Remove TP76 and TP74

10.Pull-up R103 to +1.8V_SOC_PMIC on CLK_REQ for Marvell's suggestion.

11.Electrical/Environmental Test Specification-
Add two serial resistors R409 (22ohm) between L22 and HP_OUT-L, R410 (22ohm) between L21 and HP_OUT-R.

12.Change R14.1 from +3.3V to +3.3V_NAND for sequence.

13.Using dual ext. SD power switch to support USH-I mode.

14.Reserve a cap C493 for CMD hold-timing

15.Modify MB_ID. Change R340 to 20k ohm.

16.Add a parallel cap C486(47pf) on R400 to fix SOC/EC communications issue.

17.Error key issue.
- *1.Change R386 and R392 from 0 ohm to ferrite bead(L53 and L52 with 220ohm).*
- *2.Reserve C489,C490, C491 and C492 on +VIN.*

18.Inverse the CN5.

19.Add a decoulping cap C500 (0.1uf) on HDMIC_5V and close to CN14.19

20.Fix +VIN noise
- *1.Add PC156 (10uf)on +VIN_5V_PAD.*
- *2.Add PC157 (10uf)on +VIN_3V_PAD*
- *3.Add PC155 and PC75 (10uf)on +VIN_1.8V_PAD*
- *4.Add PC104 (10uf), PC153 (10uf) and PC154(0.1uf)on +VIN_1.8V_PAD*
- *5.Add PC158 (10uf) on +VIN_DDR3_PAD.*

21. Change the conrol pin of ext. SD power discharge.

Schematic modify Item and History :

Schematic modify Item and History :

Power Plane	Voltage	Description	Control Signal	S0	S3	S5
+VADP_IN	+10.5V~+25V	Adpater In		V	V	V
+3.3VBAT	+3.0V~+3.3V	RTC		V	V	V
+3.3VSUS	+3.3V	EC POWER	+VIN	V	V	V
+5V	+5V		EN_MAIN_PWR	V	V	X
+3.3V	+3.3V	RTC	EN_MAIN_PWR	V	V	X
+10V_GATE	~+9V	+3.3V power rail gate power	EN_MAIN_PWR	V	V	X
+3.3V_SOC	+3.3V	IO power of SoC	EN_+3.3V_SOC#	V	V	X
+3.3V_USIM	+3.3V	IO power of SoC	EN_+3.3V_NAND#	V	V	X
+3.3V_SD2	+3.3V	IO power of SoC / ext. SD	EN_SD2_PWR#	V	V	X
+3.3V_NAND	+3.3V	IO power of SoC	EN_+3.3V_NAND#	V	V	X
+3.3V_BB	+3.3V	IO power of SoC	EN_+3.3V_NAND#	V	V	X
+3.3V_USB_HUB	+3.3V	USB HUB	EN_USB_PWR	V	V	X
+1.8V_PMIC	+1.8V	IO power of SoC	EN_+1.8V_PMIC#	V	V	X
+1.8V_GPIO	+1.8V	IO power of SoC	EN_+1.8V_GPIO#	V	V	X
+1.8V	+1.8V	IO power of SoC	EN_MAIN_PWR	V	V	X
+5V_USB	+1.8V	IO power of SoC / USB POWER	EN_+5V_USB#	V	V	X
+1.2V	+1.2V	IO power of SoC	EN_+1.2V	V	V	X
+1.5V_DDR3	+1.5V	Memory power	EN_+1.5V_DDR3	V	V	X
+0.75VREF_DDR3	+0.75V	Memory power	EN_+0.75V_DDR3	V	V	X
+9.6V_LCD	9.6V	Analog power for LCD	EN_LCD_PWR	V	X	X
+18V_GH	+18V	TFT on power for LCD	EN_+18V_GH	V	X	X
-7V_GL	-7V	TFT off power for LCD	EN_LCD_PWR	V	X	X
+1.8V_DCON	+1.8V	DCON	EN_DCON_PWR#	V	X	X
+2.5V_DCON	+2.5V	DCON	EN_+2.5V_DCON	V	X	X
+VCORE	+1.33~+1.40V	SoC	EN_VCORE_PWR	V	V	X
+3.3V_WLAN	+3.3V	WLAN	EN_WLAN_PWR	V	X	X
+1.8V_WLAN	+1.8V	WLAN	+3.3V_WLAN	V	X	X
+3.3V_SD1	+3.3V	eMMC	EN_SD1_PWR#	V	V	X

Title	<Title>		
Size B	Document Number NOTE		Rev 1A
Date: Wednesday, January 30, 2013	Sheet 40 of 40		