XO-3 EC Pin Assignments

Pin	Special Func.	GPIO	Reset strap ?	ECRST# (L/H)	XO-3 (CL3) Signal Name	XO-3 Dir	XO-1.75 (CL2) Signal Name	XO-1.75 Dir	Description (XO-3)
1	KSI6 / EDI_DI	GPIO00		IE(PU) / IE(PU)	EDI_DIN_R	I	EDI_DIN_R	I	SOC/ISP programming interface
2	KSI7 / EDI_DO	GPIO01		IE(PU) / IE(PU)	EDI_DO_R	O	EDI_DO_R	O	SOC/ISP programming interface
3	KSO4	GPIO02		IE(PU) / IE(PU)	SOC_RESET#	O	SOC_RESET#	O	Open drain SOC reset, not system reset
4	KSO5	GPIO03		IE(PU) / IE(PU)	PWR_LMT_ON#	I	PWR_LMT_ON#	I	Low-end (solar) power limiting active
5	KSO6	GPIO04	H	IE(PU) / IE(PU)	EN_+1.8V_GPIO#	O	EN_+1.8V_GPIO#	O	Enable +1.8V_GPIO
6	KSO7	GPIO05		HiZ / HiZ	EN_USB_PWR	O	EN_USB_PWR	O	Enable +3.3V_USB to USB Hub
7	OWM	GPIO06		HiZ / HiZ	CHRG_DQ	I/O	CHRG_DQ	I/O	Battery 1-Wire interface
8	PWM1	GPIO07		HiZ / HiZ	LED_BAT_R	O	LED_BAT_R	O	Battery LED Red
9	AD0	GPI08		HiZ / HiZ	EC_ID0	AI	EC_ID0	AI	Board ID 0
10	AD1	GPI09		HiZ / HiZ	EC_ID1	AI	EC_ID1	AI	Board ID 1
11	AD2	GPI0A		HiZ / HiZ	CHRG_AC_IN	AI	CHRG_AC_IN	AI	Voltage at DC Line In
12	AD3	GPI0B		HiZ / HiZ	CHRG_USB_IN	AI	SOC_SLEEP	I	Voltage on USB power pin
13	AD4	GPI0C		HiZ / HiZ	ADP_CUR_SEN	AI	ADP_CUR_SEN	AI	Adapter current sense
14	AD5	GPI0D		HiZ / HiZ	CHRG_VOL_SNS	AI	CHRG_VOL_SNS	AI	Main rail voltage sense
15	*AVCC*								
16	DA0	GPO0E		HiZ / HiZ	*TP45*	AO/O	*TP172*	AO/O	
17	DA1	GPO0F		HiZ / HiZ	*TP46*	AO/O	*TP173*	AO/O	
18	*AGND*								
19	SPI_CLK	GPIO10		HiZ / IE	SDI_CLK	I	SDI_CLK	I	EC ↔ SOC Communication
20	SPI_DO	GPIO11		HiZ / IE	SDI_MOSI	O	SDI_MOSI	O	EC ↔ SOC Communication
21	SPI_DI	GPIO12		HiZ / IE	SDI_MISO	I	SDI_MISO	I	EC ↔ SOC Communication
22	SPI_CS#	GPIO13		HiZ / IE	SDI_CS#	I	SDI_CS#	I	EC ↔ SOC Communication
23	*NC*								
24	*VCC*								
25	PWM0	GPIO14		HiZ / HiZ	OLS_ANODE	O	OLS_ANODE	O	Outdoor Light Sensor anode
26	PWM2	GPIO15		HiZ / HiZ	LV_SET	O	LV_SET	O	MPPT low-end setpoint control
27	PWM3	GPIO16		HiZ / HiZ	LED_BAT_G	O	LED_BAT_G	O	Battery LED Green
28	CEC	GPIO17		HiZ / HiZ	EN_VCORE_PWR	O	EN_VCORE_PWR	O	Enable SOC core power
29	CIRRX / KSO16	GPIO18		HiZ / HiZ	EC_IRQ#	O	EC_IRQ#	O	EC interrupt to the SOC
30	DS0	GPIO19		HiZ / HiZ	LED_PWR	O	LED_PWR	O	Power LED
31	DS1	GPIO1A		HiZ / HiZ	*n.c.*	I/O	EN_DCON_PWR#	O	
32	CIRTX / KSO17	GPIO1B		HiZ / HiZ	SYS_RESET#	I	SYS_RESET#	I	System reset input
33	IRQ#	GPIO1C		PU / PU	ALL_PWRGD	I	ALL_PWRGD	I	System power good input
34	RX	GPIO1D		HiZ / HiZ	EC_RX	I	EC_RX	I	UART In
35	TX	GPIO1E		HiZ / HiZ	EC_TX	O	EC_TX	O	UART Out
36	RESET#			IE / IE	EC_RST#	I	EC_RST#	I	EC reset
37	KSO0	GPIO1F	H	IE(PU)/IE(PU)	EN_+1.8V_PMIC#	O	EN_+1.8V_PMIC#	O	Enable +1.8V_PMIC
38	KSO1	GPIO20	H	IE(PU)/IE(PU)	*n.c.*	I/O	EN_SD1_PWR#	O	
39	KSO2	GPIO21	H	IE(PU)/IE(PU)	*n.c.*	I/O	EN_SD2_PWR#	O	
40	KSO3	GPIO22	H	IE(PU)/IE(PU)	EN_+3.3V_SOC#	O	EN_+3.3V_SOC#	O	Enable +3.3V_SOC
41	KSO8	GPIO23		HiZ / HiZ	CHRG_AC_OK	I	CHRG_AC_OK	I	External DC Input present
42	KSO9	GPIO24		HiZ / HiZ	EN_MAIN_PWR	O	EN_MAIN_PWR	O	Enable main power plane
43	KSO10	GPIO25		HiZ / HiZ	EC_SPI_ACK	O	EC_SPI_ACK	O	EC->SOC command acknowledge
44	KSO11	GPIO26		HiZ / HiZ	EN_+3.3V_NAND#	O	EN_+3.3V_NAND#	O	Enable +3.3V_NAND

XO-3 EC Pin Assignments

Pin	Special Func.	GPIO	Reset strap ?	ECRST# (L/H)	XO-3 (CL3) Signal Name	XO-3 Dir	XO-1.75 (CL2) Signal Name	XO-1.75 Dir	Description (XO-3)
45	KSO12	GPIO27		HiZ / HiZ	EN_+1.5V_DDR3	O	EN_+1.5V_DDR3	O	Enable +1.5V_DDR3
46	KSO13	GPIO28		HiZ / HiZ	EN_+1.2V	O	EN_+1.2V	O	Enable +1.2V
47	KSO14	GPIO29		HiZ / HiZ	*n.c.*	O	OLS#	O	
48	KSO15	GPIO2A		HiZ / HiZ	PWR_BTN#	I	PWR_BTN#	I	Input from power button
49	CLK_IN				EC_XTL_IN	AI	EC_XTL_IN	AI	32KHz crystal connection
50	CLK_OUT				EC_XTL_OUT	AO	EC_XTL_OUT	AO	32KHz crystal connection
51	SDA0	GPIO2D		HiZ / IE	CHG_SDA	I/O	CHG_SDA	I/O	Battery Charger SMBus interface data
52	SCL0	GPIO2E		HiZ / IE	CHG_SCL	I/O	CHG_SCL	I/O	Battery Charger SMBus interface clock
53	KSI2	GPIO2F		IE(PU)/IE(PU)	EC_SPI_CMD	I	EC_SPI_CMD	I	SOC->EC command flag
54	KSI3	GPIO30		IE(PU)/IE(PU)	OLS_CATHODE	I/O	OLS_CATHODE	I/O	Outdoor Light Sensor cathode
55	KSI0	GPIO31		IE(PU)/IE(PU)	RESTORE	I	RESTORE	I	Enable EC recovery mode
56	KSI1	GPIO32		IE(PU)/IE(PU)	SOC_SLEEP	I	EN_KBD_PWR#	O	Indicator that the main proc. is asleep
57	KSI4 / EDI_CS	GPIO33		IE(PU)/IE(PU)	EDI_CS_R#	I	EDI_CS_R#	I	SOC/ISP programming interface
58	KSI5 / EDI_CLK	GPIO34		IE(PU)/IE(PU)	EDI_CLK_R	I	EDI_CLK_R	I	SOC/ISP programming interface
59	SDA1 / PS2_DAT3	GPIO35		HiZ / HiZ	*n.c.*	I/O	TPD_DAT	I/O	
60	*VCC*								
61	SCL1 / PS2_CLK3	GPIO36		HiZ / HiZ	*n.c.*	I/O	TPD_CLK	I/O	
62	*GND*								
63	PS2_CLK1	GPIO37		HiZ / HiZ	*n.c.*	I/O	KBD_CLK	I/O	
64	PS2_DAT1	GPIO38		HiZ / HiZ	*n.c.*	I/O	KBD_DAT	I/O	

HiZ – High impedance
IE – Input enabled
IE(PU) – Input enabled w. internal pullup